

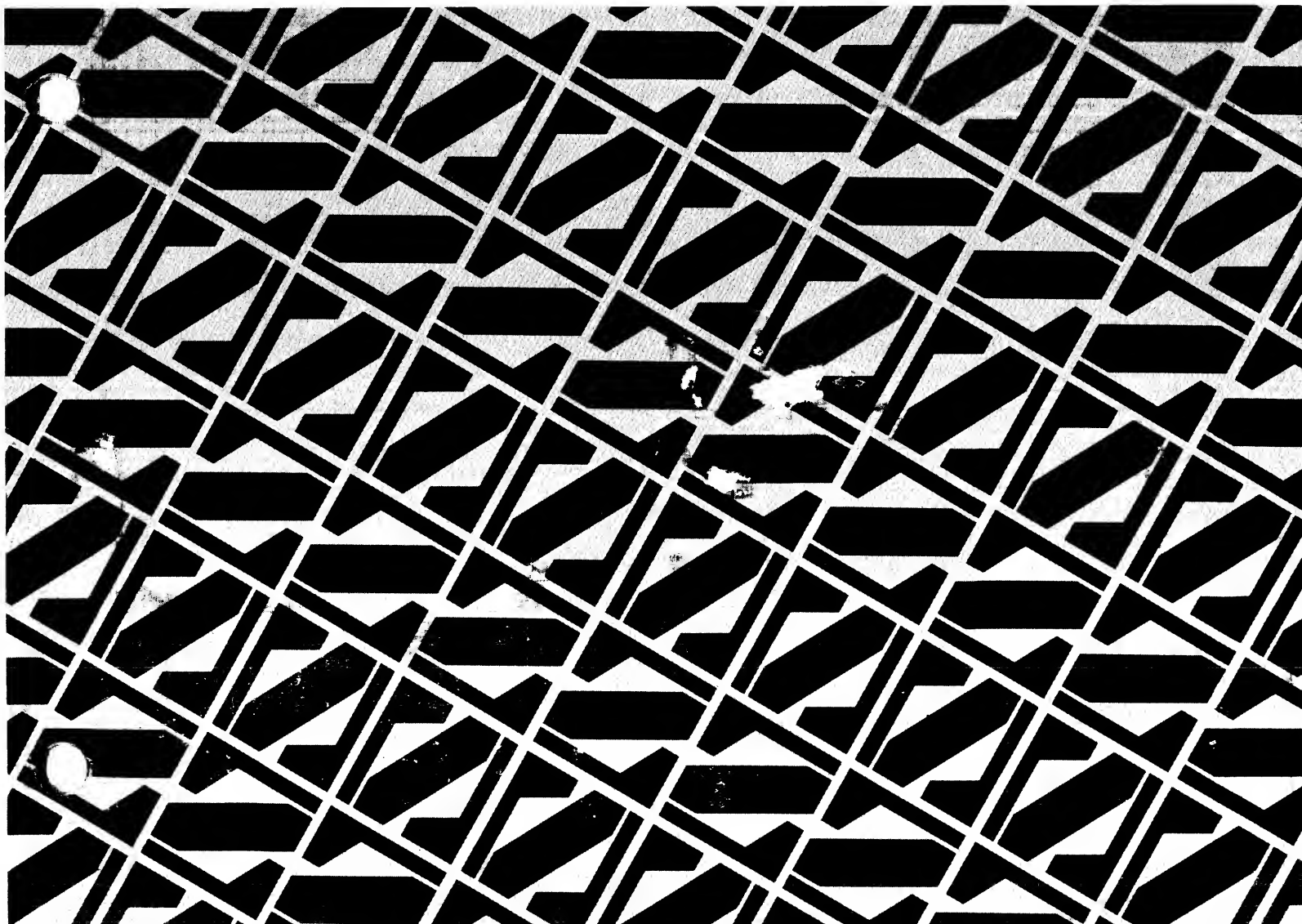
National Semiconductor

Order No. IMP-16P/937A

Pub. No. 4200037A

IMP-16P Users Manual

Volume 2



Order Number IMP-16P/937A
Publication Number 4200037A

IMP-16P MICROCOMPUTER

IMP-16P
USERS MANUAL
VOLUME 2

October 1974

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2900 Semiconductor Drive
Santa Clara, California 95051

PREFACE

Volume 2 of the IMP-16P Users Manual contains detailed block, timing, and schematic diagrams to assist the user in tutorial or maintenance endeavors. The detailed functional descriptions contained in volume 1, chapter 7, of this manual are written to the detailed functional block and timing diagrams contained in volume 2. The small numbers within squares located in the functional blocks of the block diagrams designate the associated schematic sheet number.

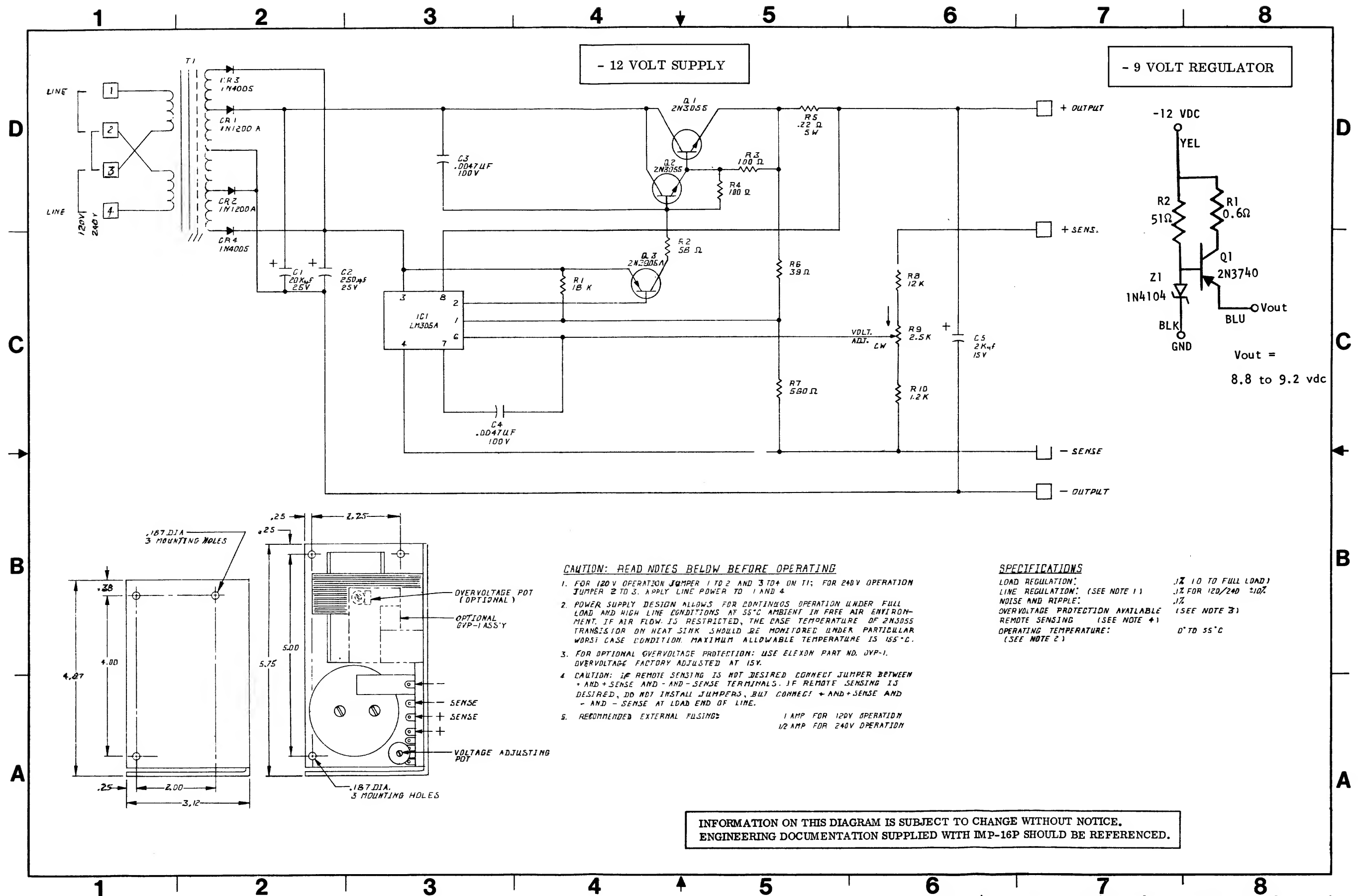
Appendix A is a list of all mnemonics used in both volumes 1 and 2. Appendix B is a compilation of the circuit diagrams of the various devices appearing in the schematic diagrams of the IMP-16P. Appendixes A and B follow the illustrations in volume 2.

The material in this manual is subject to change without notice. Circuit details and other data supplied with the engineering documentation that accompany equipment take precedence over the information contained in this manual.

Copies of this manual and other National Semiconductor publications may be obtained from the sales offices listed on the back cover.

CONTENTS

Figure		Page
2/6-1	Power Supplies Schematic Diagram	2/6-1
2/7-1	IMP-16C Functional Block Diagram	2/7-1
2/7-2	IMP-16C Schematic Diagram	2/7-2
2/7-3	Memory Timing Diagram	2/7-6
2/7-4	Memory Timing and Control Card Functional Block Diagram	2/7-7
2/7-5	Memory Timing and Control Card Schematic Diagram	2/7-8
2/7-6	Memory Storage Card Functional Block Diagram	2/7-11
2/7-7	Memory Storage Card Schematic Diagram	2/7-12
2/7-8	TTY/Card Reader Interface Card Functional Block Diagram	2/7-15
2/7-9	TTY/Card Reader Interface Card Schematic Diagram	2/7-17
2/7-10	Programmers Panel Card Schematic Diagram	2/7-21
2/7-11	Operators Control Panel Schematic Diagram	2/7-23
2/7-12	Control Panel Interface Card Functional Block Diagram	2/7-24
2/7-13	Control Panel Interface Card Timing Diagram	2/7-25
2/7-14	Control Panel Interface Card Schematic Diagram	2/7-27
APPENDIX A	LIST OF MNEMONICS/ABBREVIATIONS	2/A-1
APPENDIX B	INTEGRATED CIRCUIT DEVICE DIAGRAMS	2/B-1



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Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 1 of 4)
2/6-1

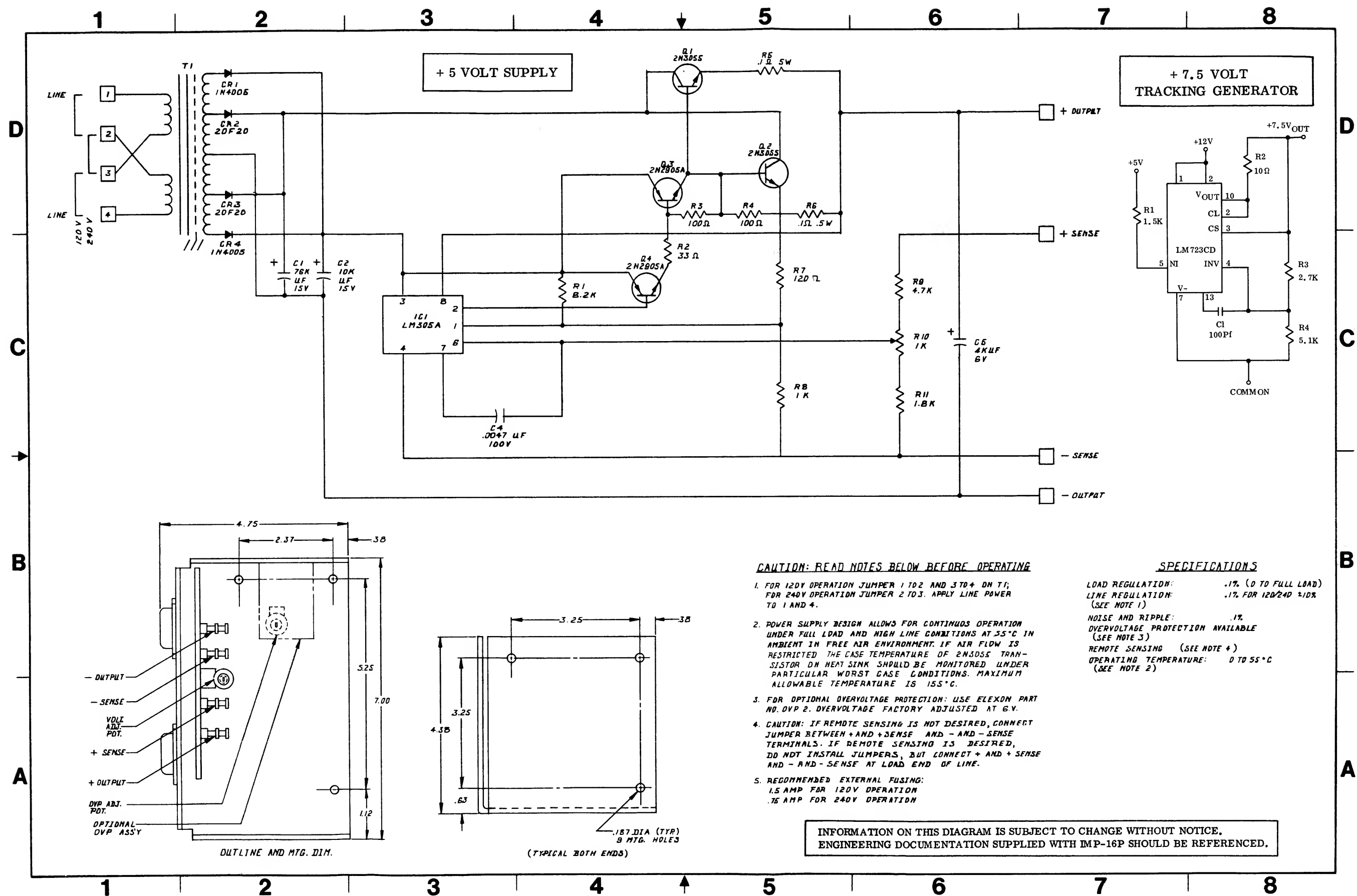


Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 2 of 4)
2/6-2

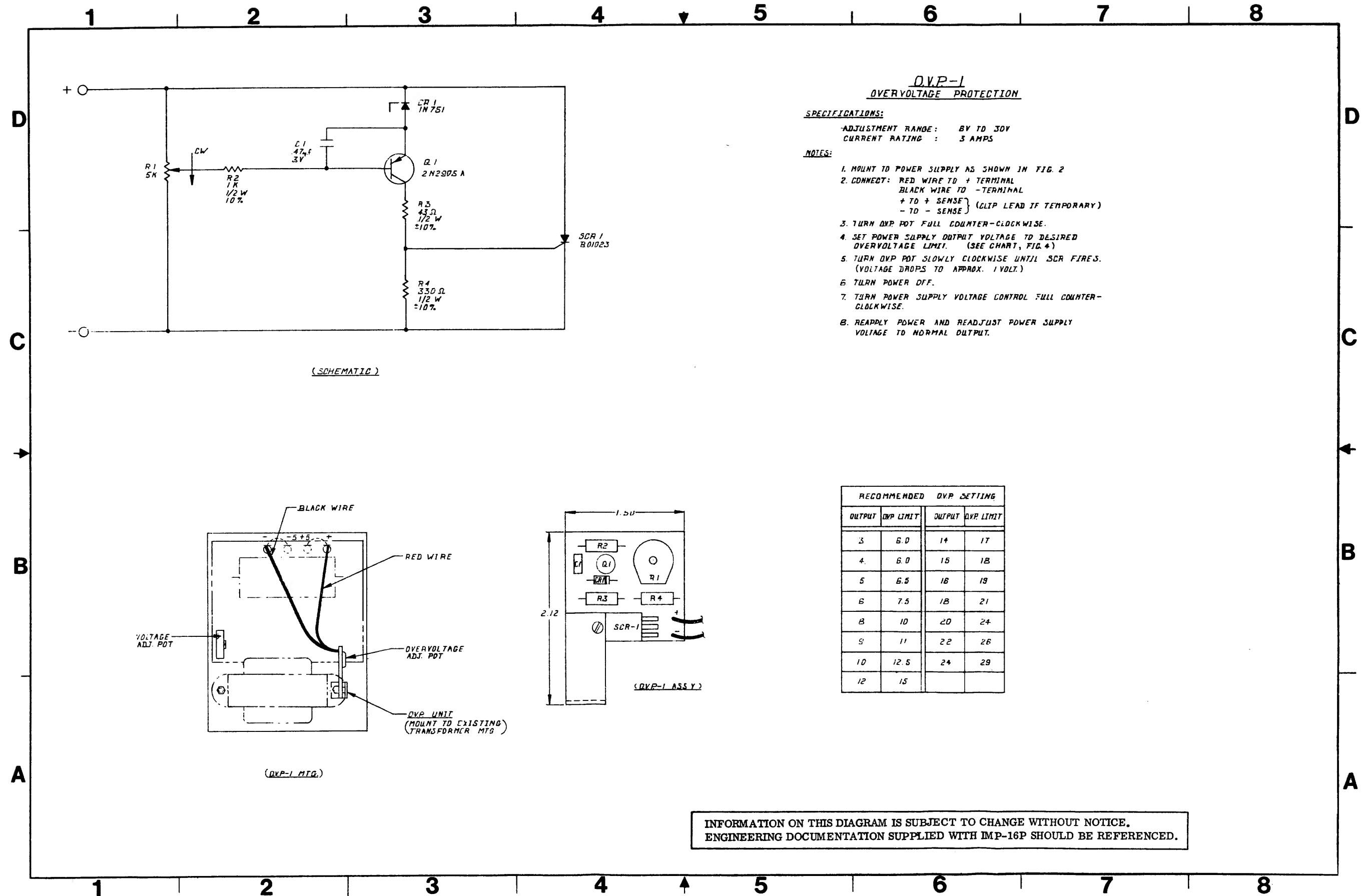


Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 3 of 4)

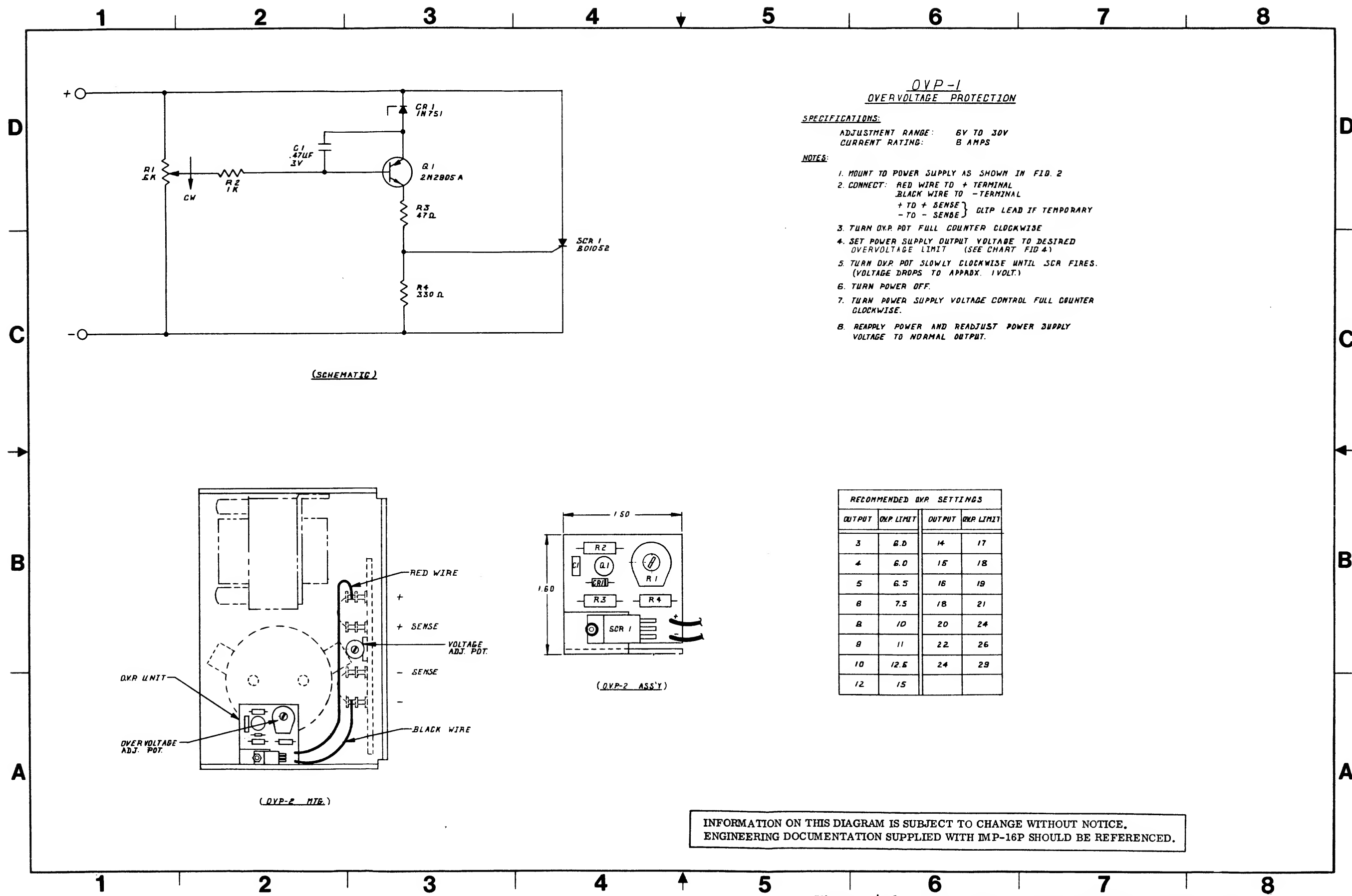
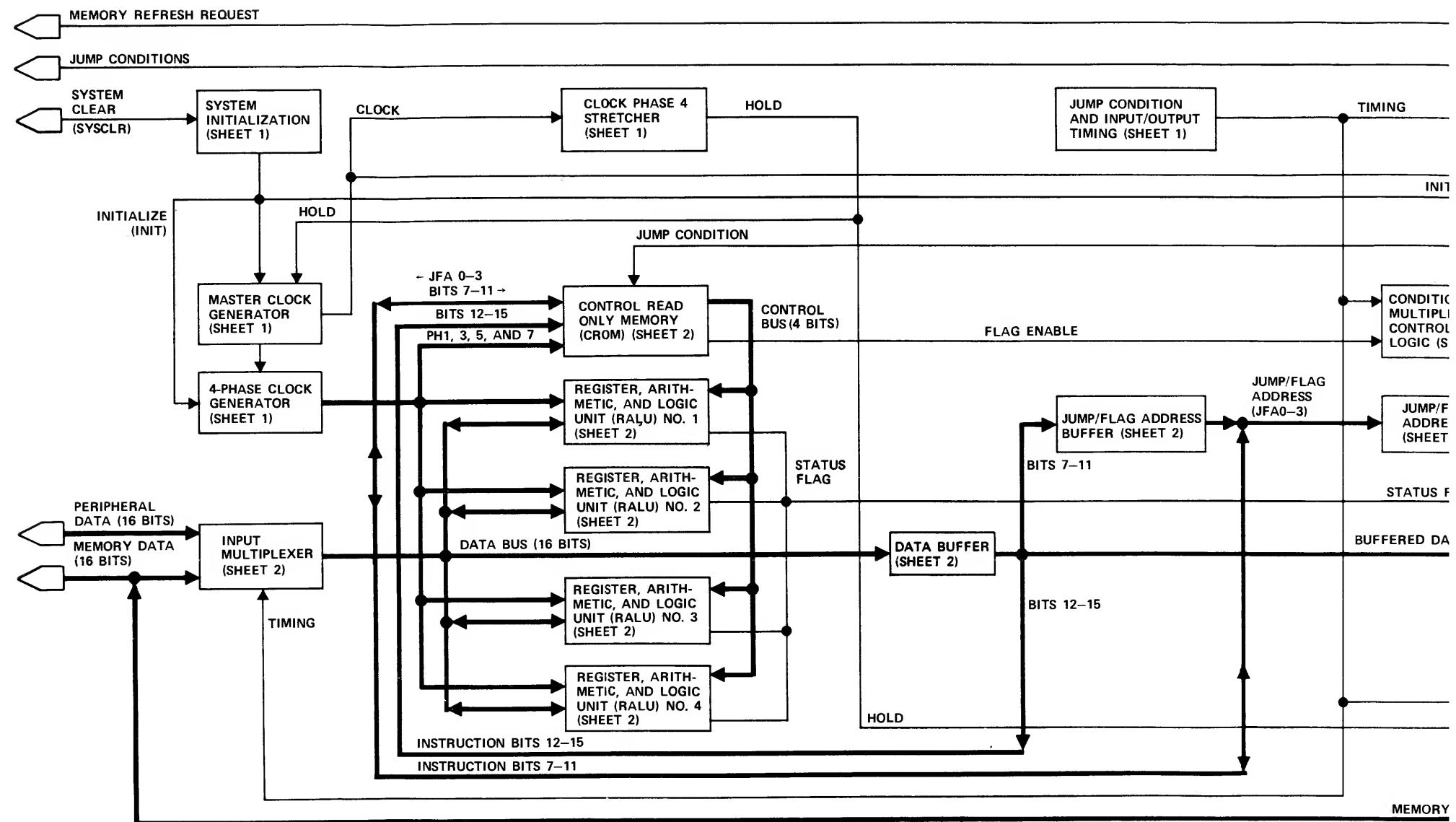
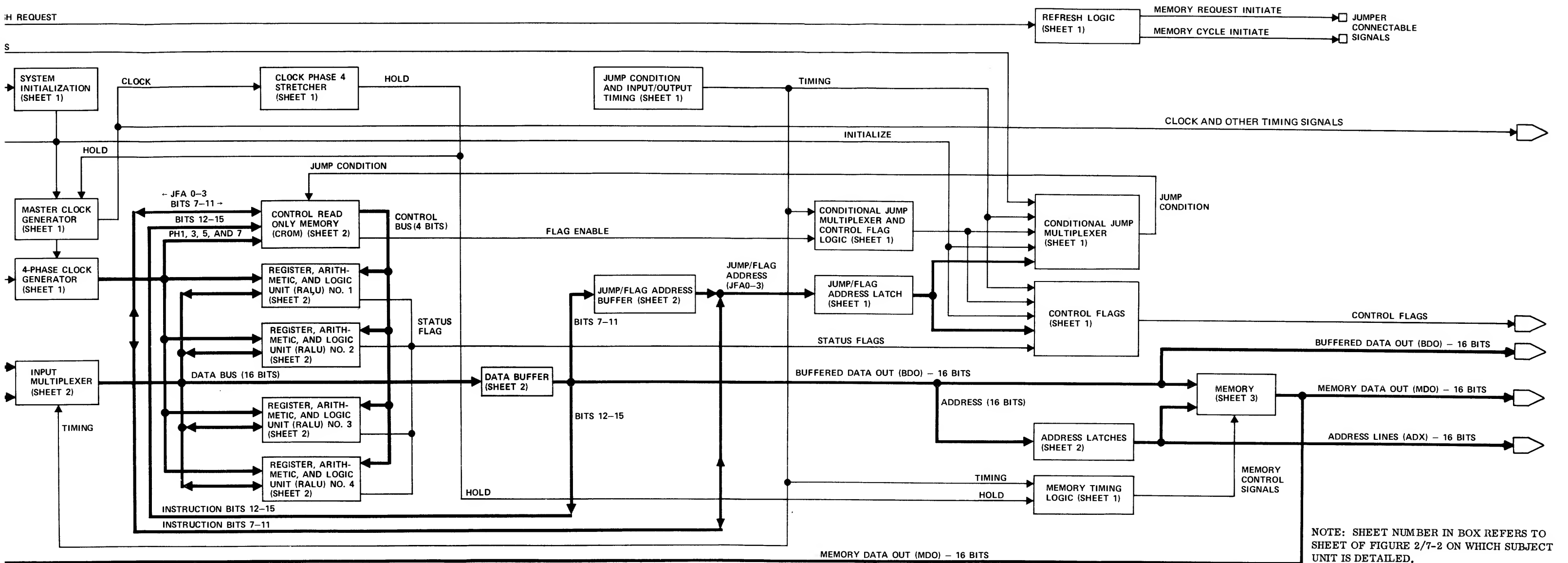


Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 4 of 4)
2/6-4



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Figure 2/7-1. IMP-16C Functional Block Diagram
2/7-1

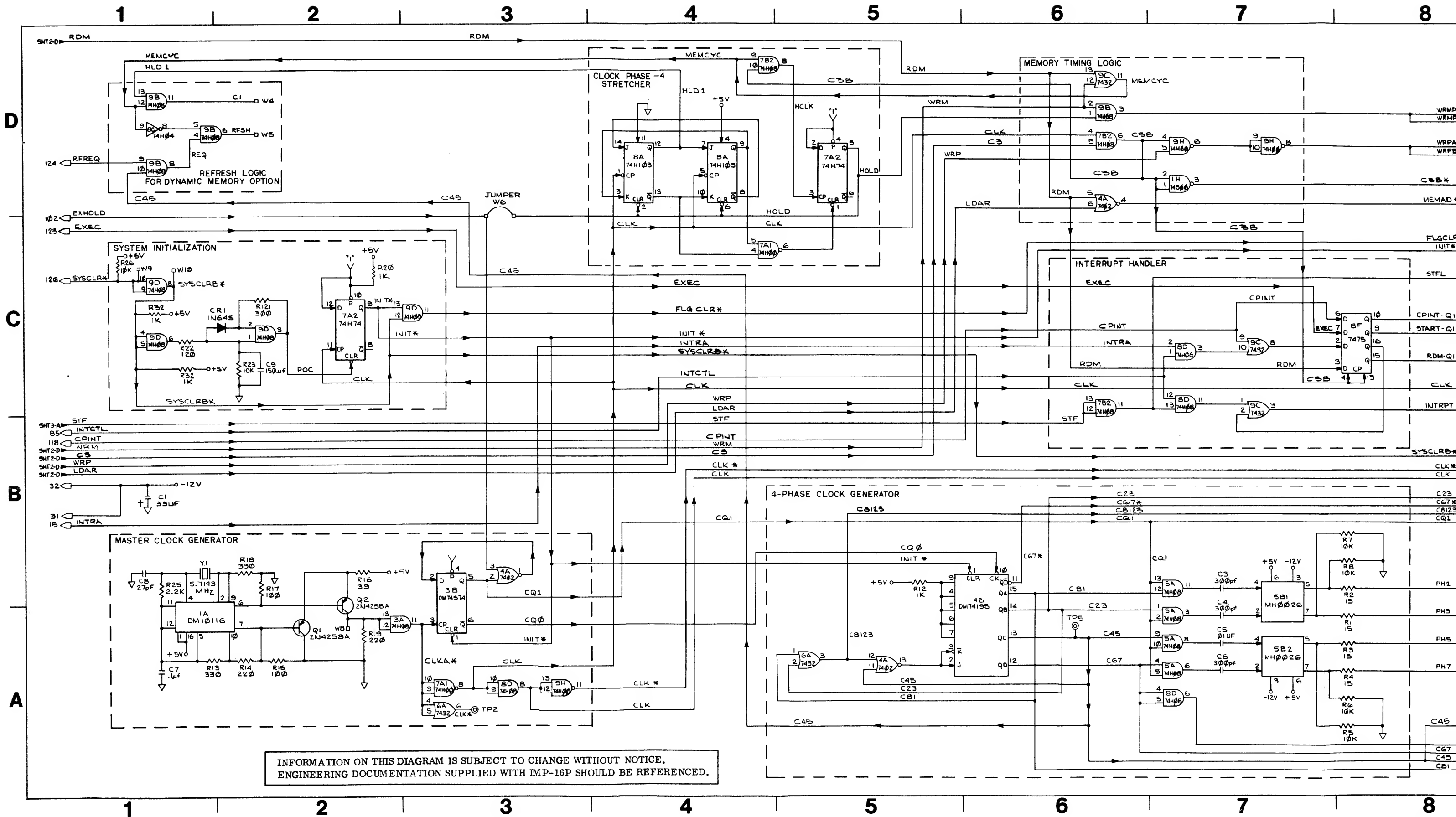


Figure 2/7-2.

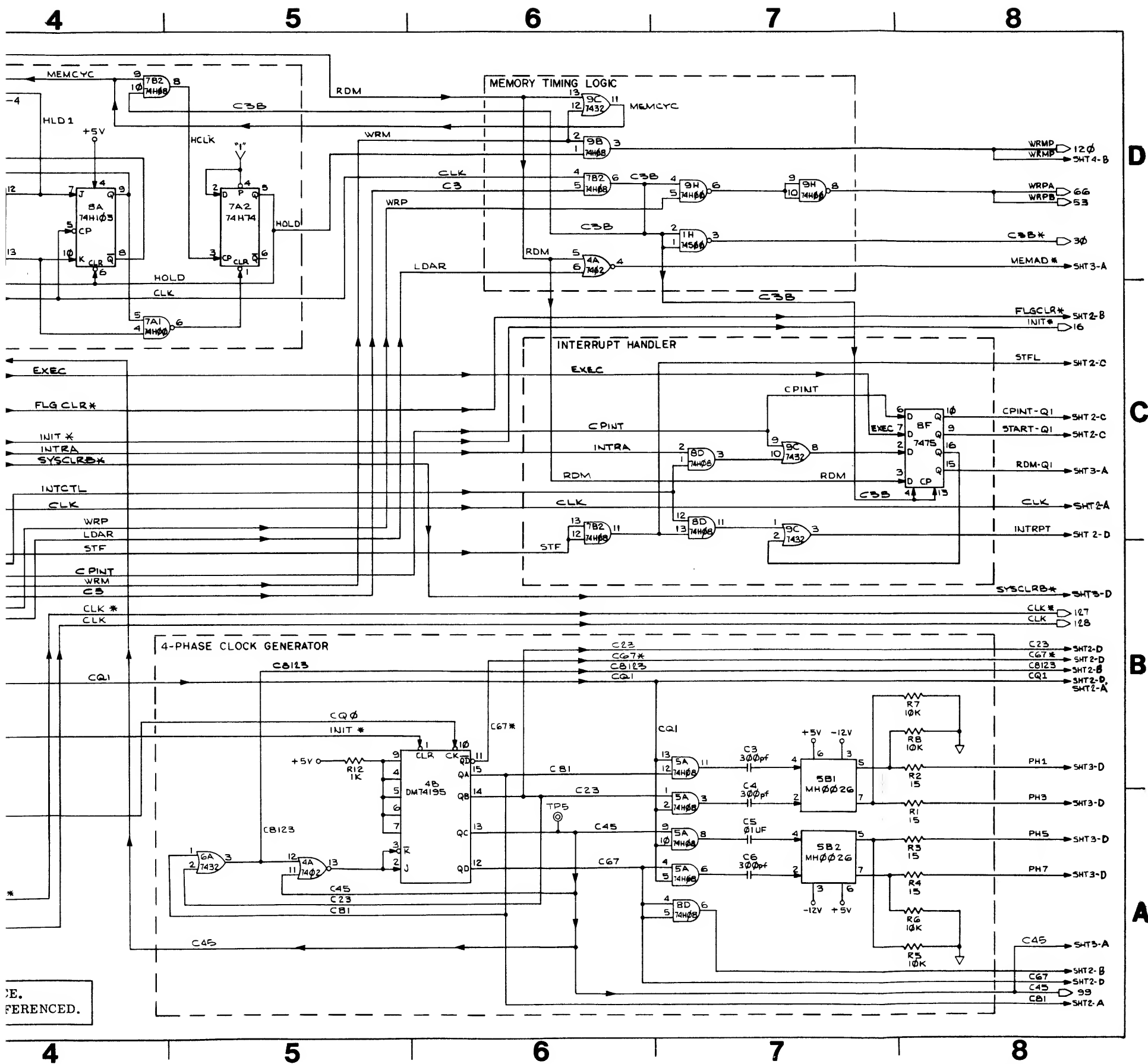


Figure 2/7-2. IMP-16C Schematic Diagram
(Sheet 1 of 4)
2/7-2

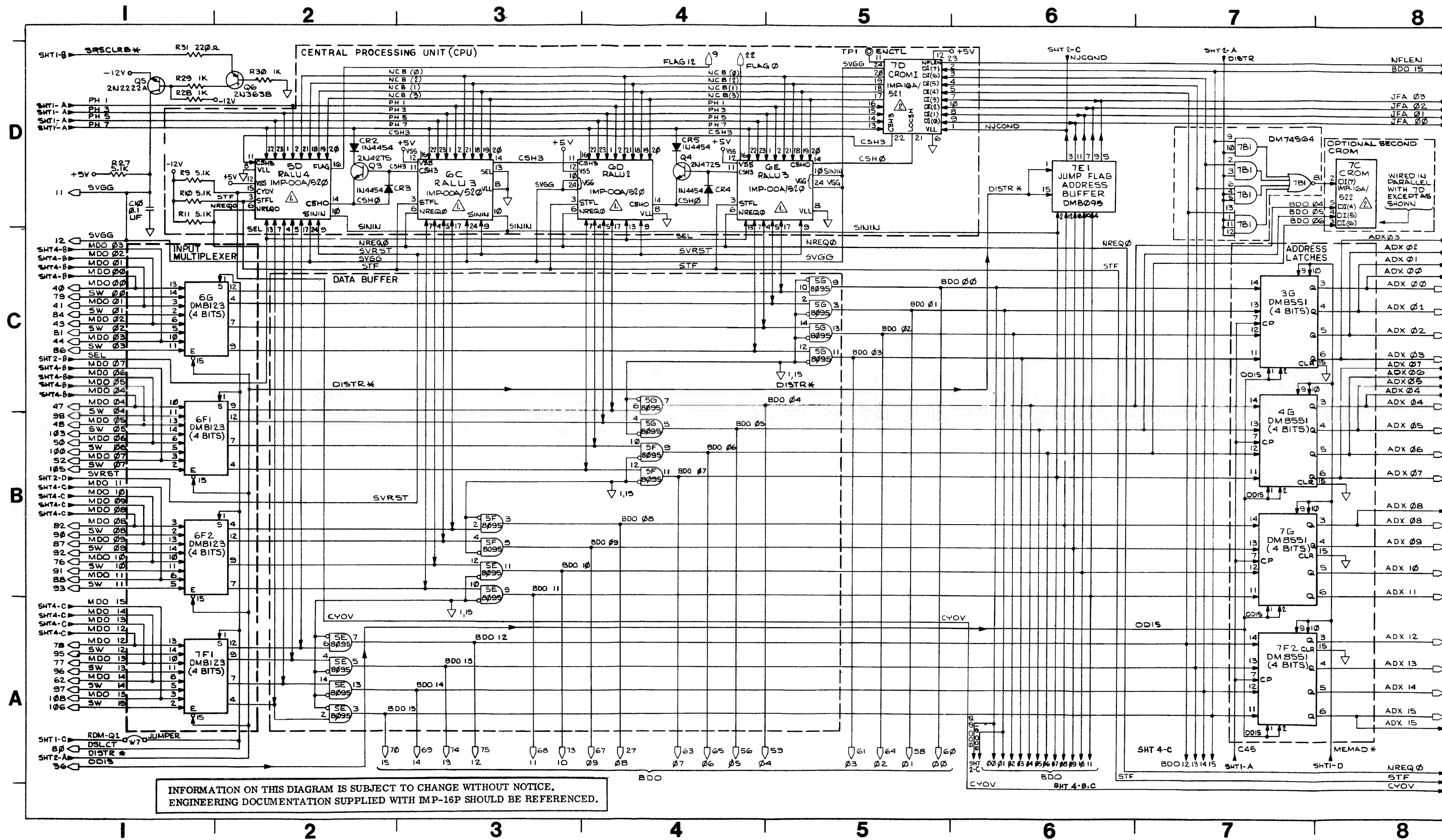


Figure 2/7-2.

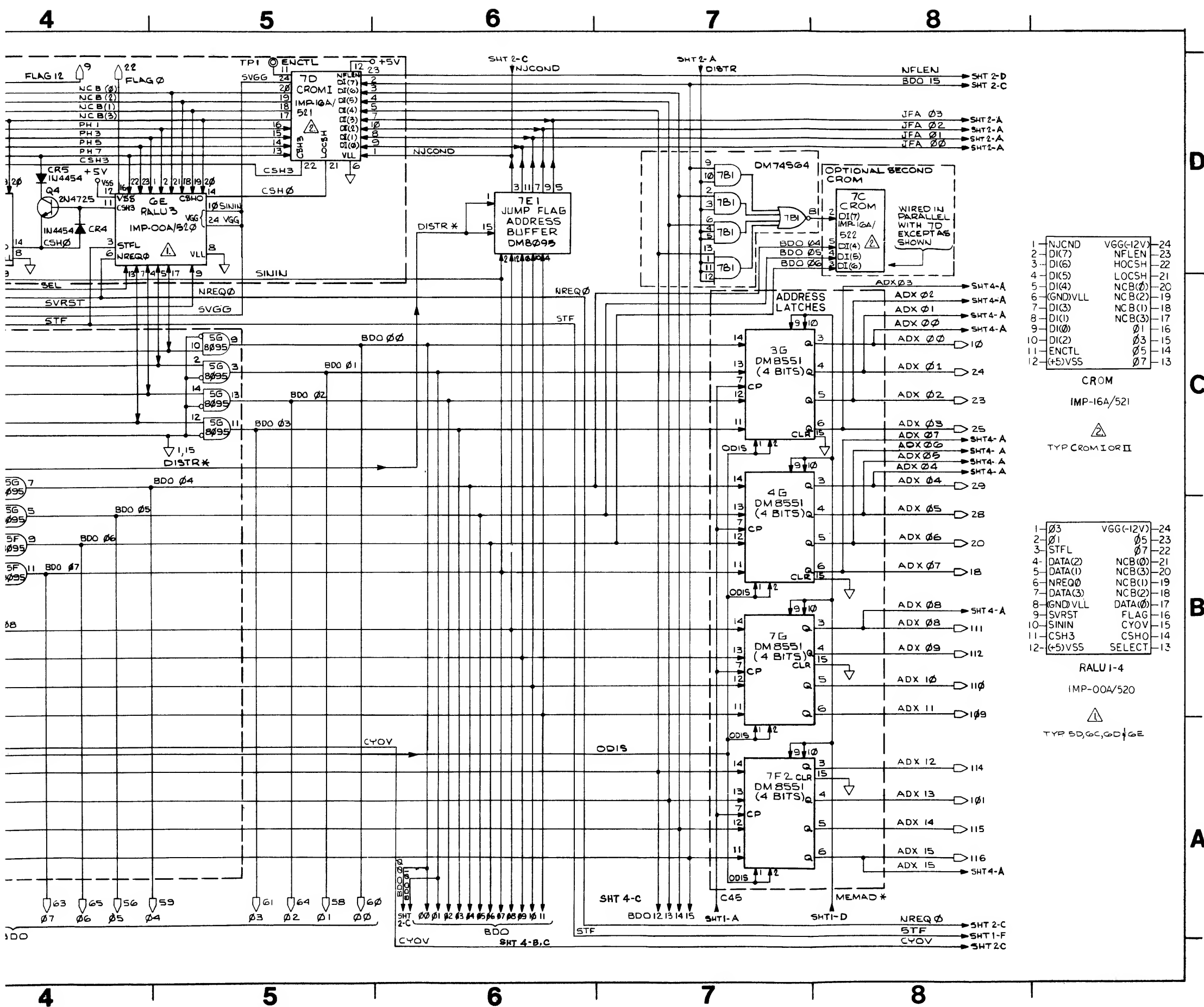
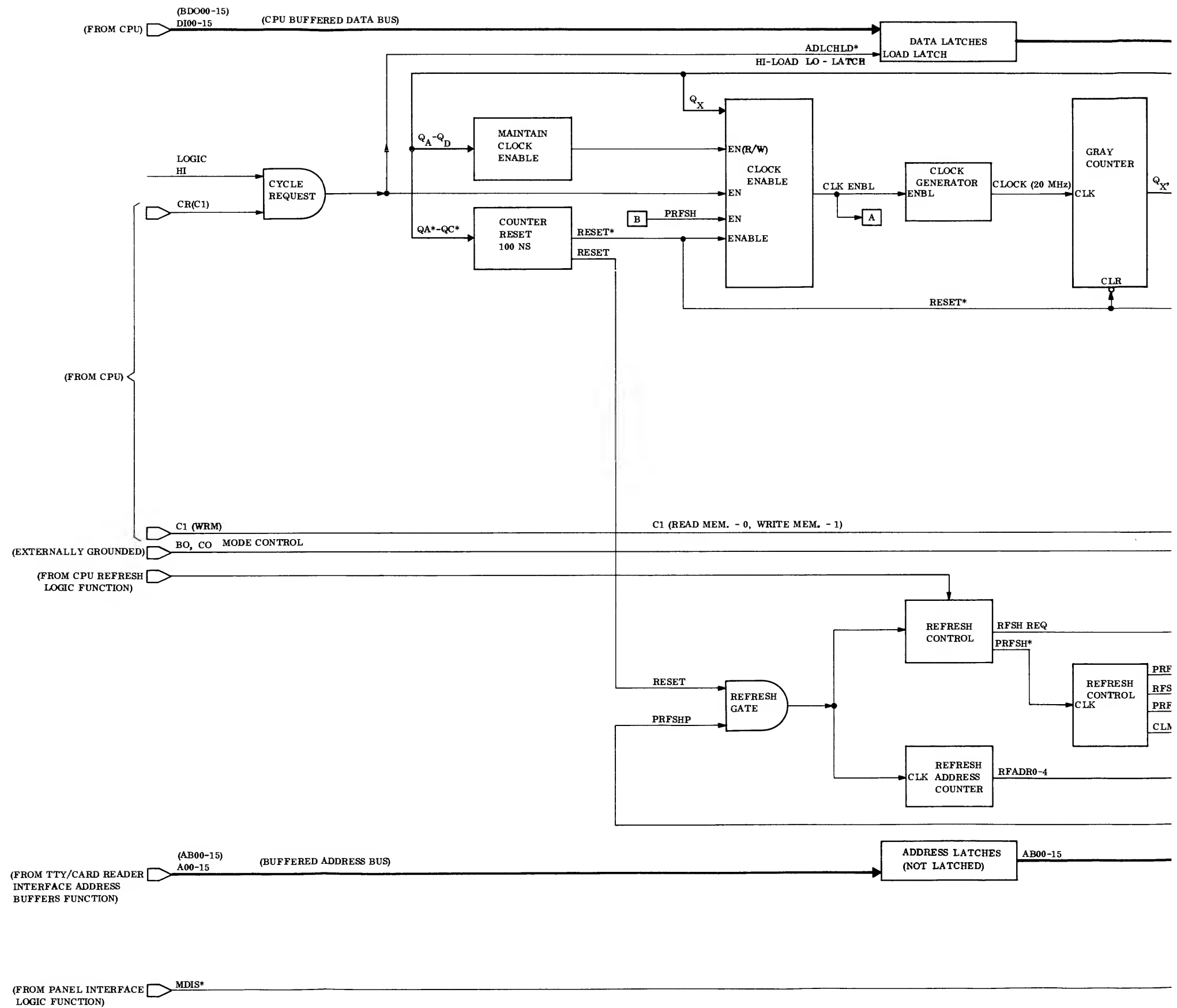


Figure 2/7-2. IMP-16C Schematic Diagram
(Sheet 3 of 4)
2/7-4



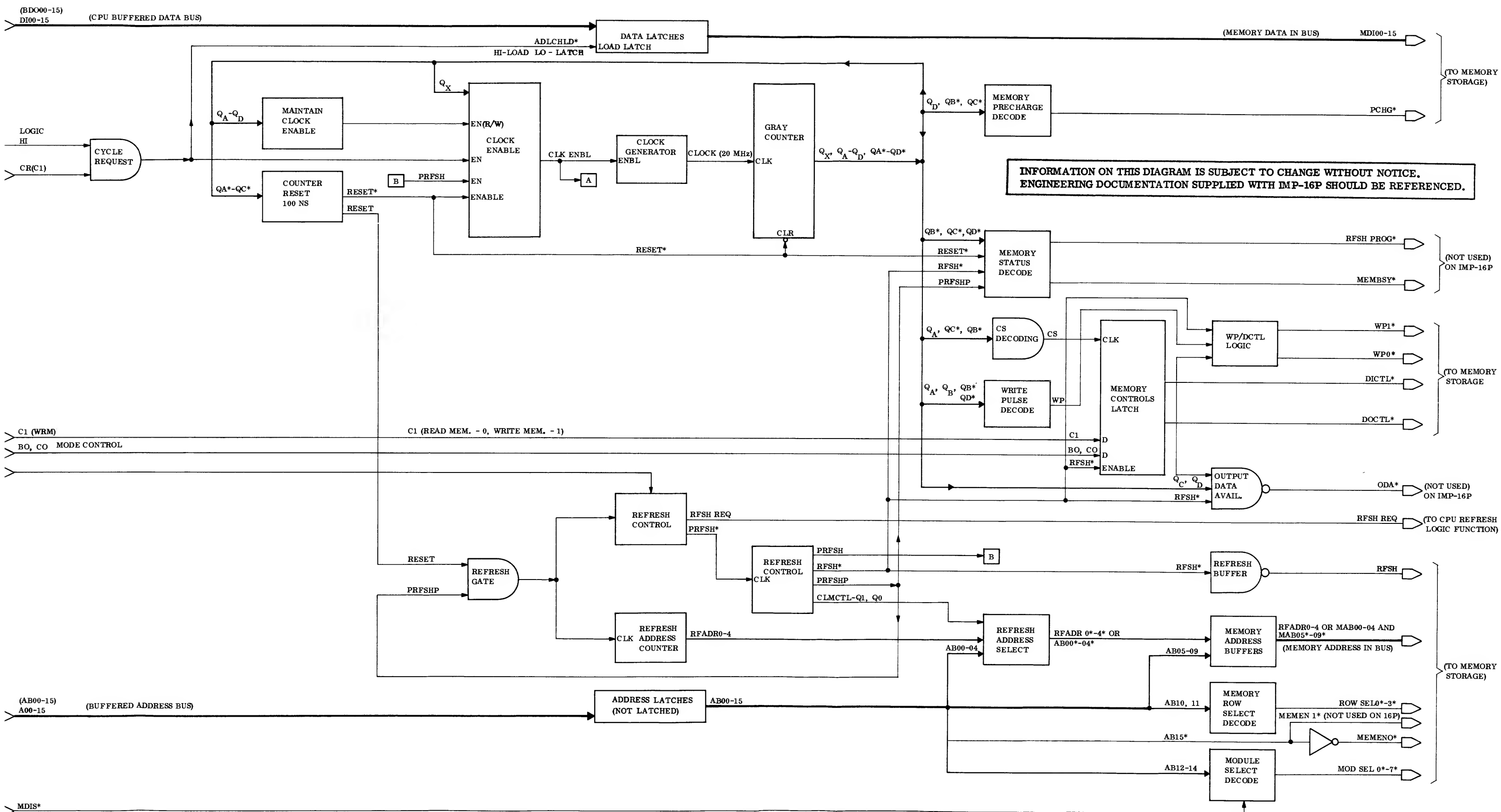
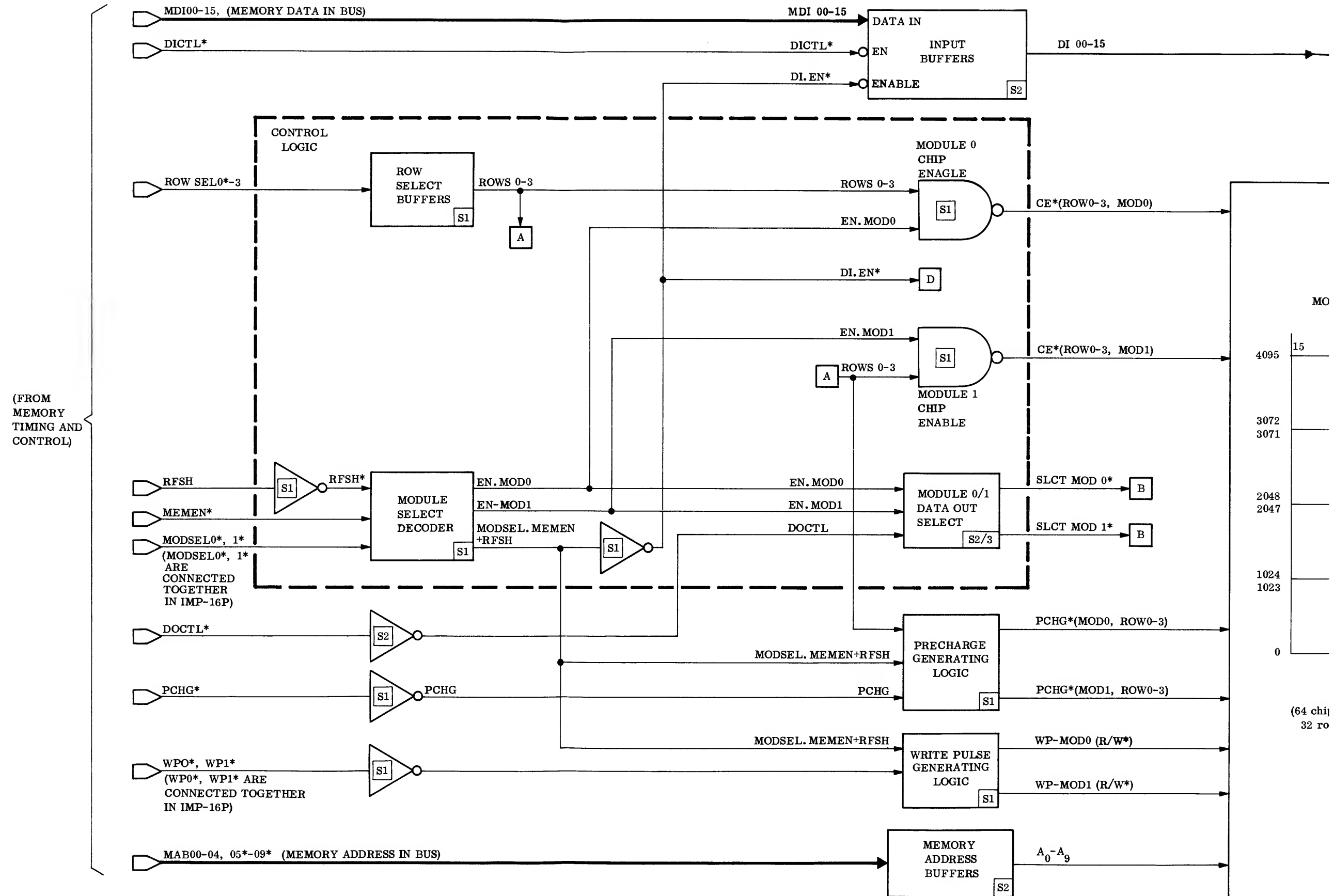
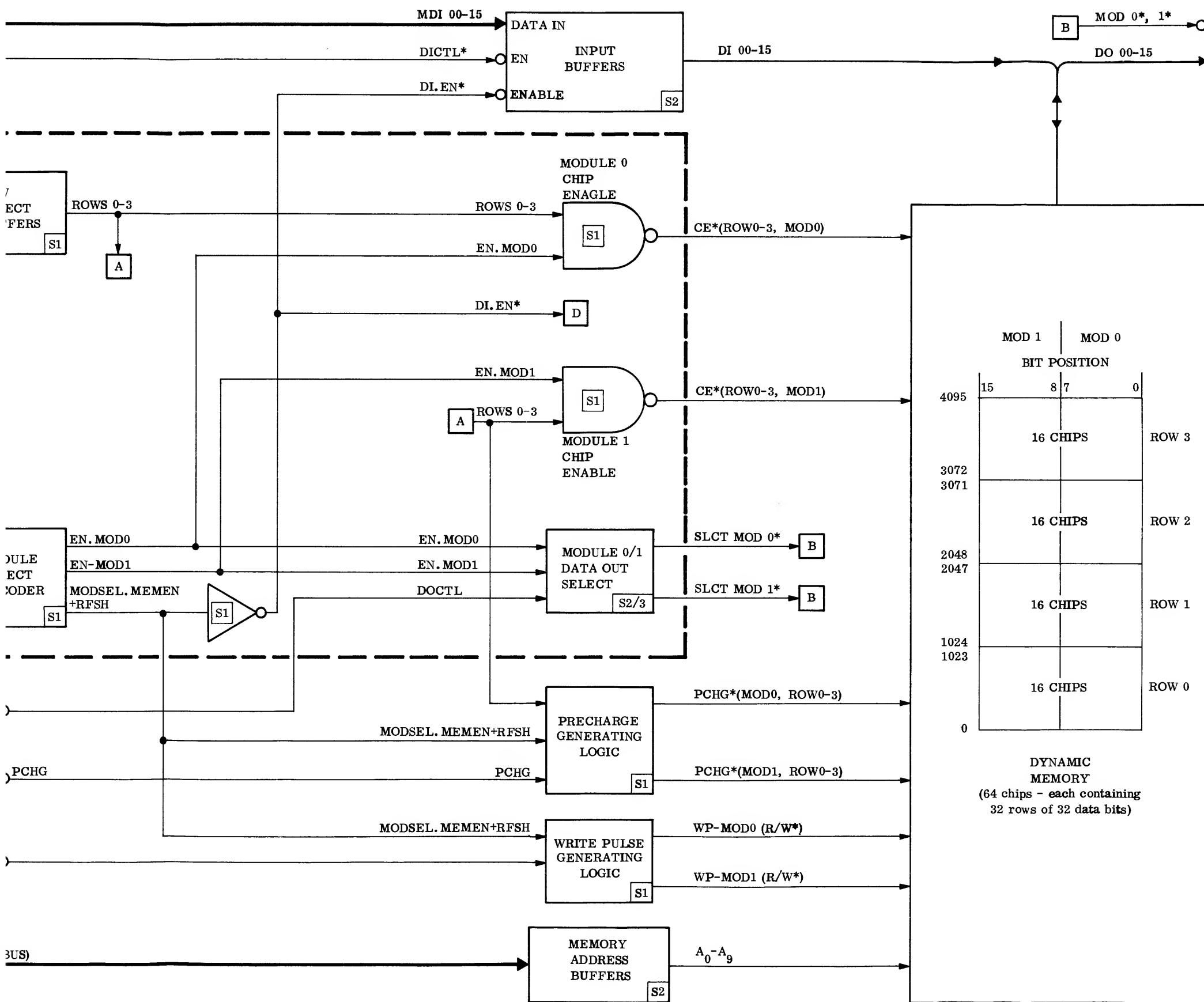


Figure 2/7-4. Memory Timing and Control Card
Functional Block Diagram
2/7-7





DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS

MNEMONIC/ABBREVIATION	DEFINITION
A0 - A9	ADDRESS BITS 0-9
CE	CHIP ENABLE
DI 00-15	DATA IN BITS 00-15
DICTL	DATA IN CONTROL
DI. EN	DATA IN ENABLE
DO 00-15	DATA OUT BITS 00-15
DOCTL	DATA OUT CONTROL
EN, MOD 0, 1	MEMORY ENABLE AND MODULE SELECT 0, 1
MAB 00-09	MEMORY ADDRESS BITS 00-09
MDO 00-15	MEMORY DATA OUT BITS 00-15
MDI 00-15	MEMORY DATA IN BITS 00-15
MEMEN	MEMORY ENABLE
MOD SEL 0, 1	MODULE SELECT 0, 1
PCHG	PRECHARGE
RFSH	REFRESH
R/W (MOD 0, 1)	READ/WRITE (MODULE 0, 1)
ROW SEL 0-3	ROW SELECT 0-3
WP 0, 1	WRITE PULSE 0, 1
EN. OUT. MOD 0/1	ENABLE OUTPUT OF MOD 0/1

NOTES:

1. MODULE 0 IS RIGHT (OR LEAST SIGNIFICANT HALF OF 16-BIT WORD)
2. MODULE 1 IS LEFT (OR MOST SIGNIFICANT HALF OF 16-BIT WORD)
3. ROW 0 IS 1st 1024 ADDRESSES

1
↓
2

2nd
↓
3rd

1024 ADDRESSES
↓
1024 ADDRESSES

 ROW 3 IS 4th 1024 ADDRESSES
4. '*' DENOTES NEGATIVE TRUE SIGNAL STATE
5. NUMBERS WITHIN SQUARES LOCATED IN LOWER RIGHT-HAND CORNER OF FUNCTIONS REFER TO ASSOCIATED SCHEMATIC SHEET NUMBERS.

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Figure 2/7-6. Memory Storage Card Functional Block Diagram
2/7-11

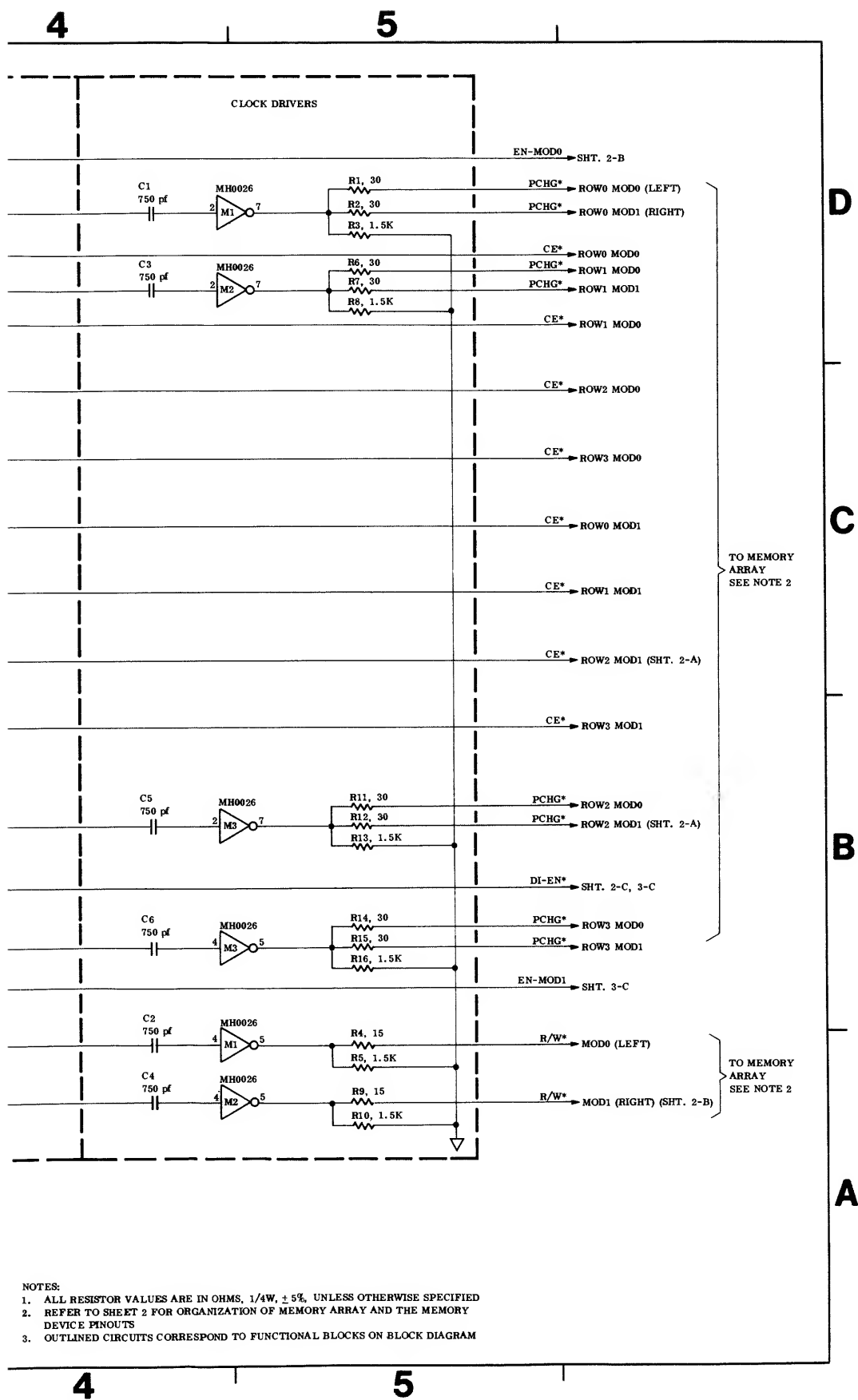


Figure 2/7-7. Memory Storage Card Schematic Diagram (Sheet 1 of 3)
2/7-12

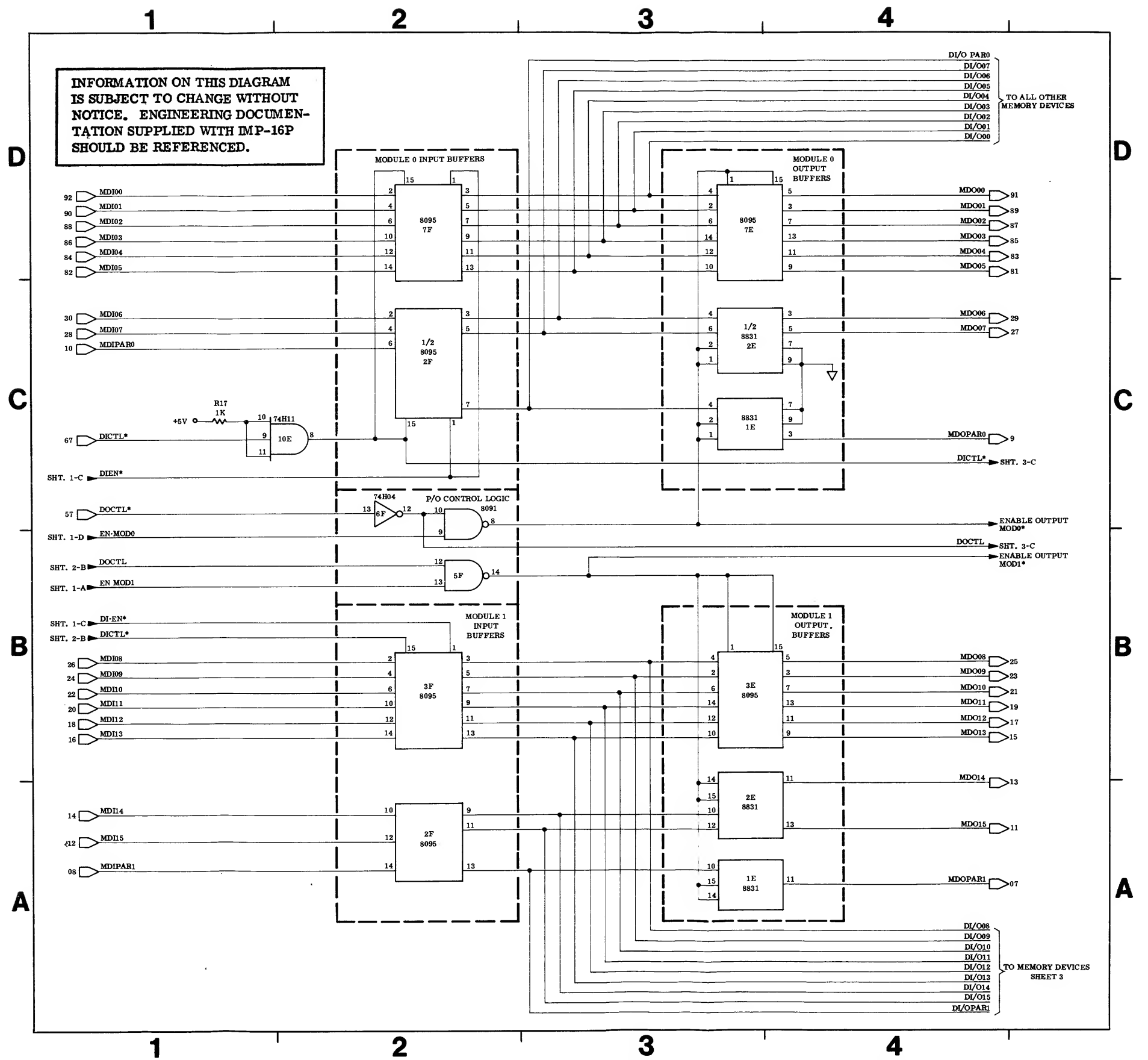


Figure 2/7-7. Memory Storage Card Schematic Diagram (Sheet 2 of 3)

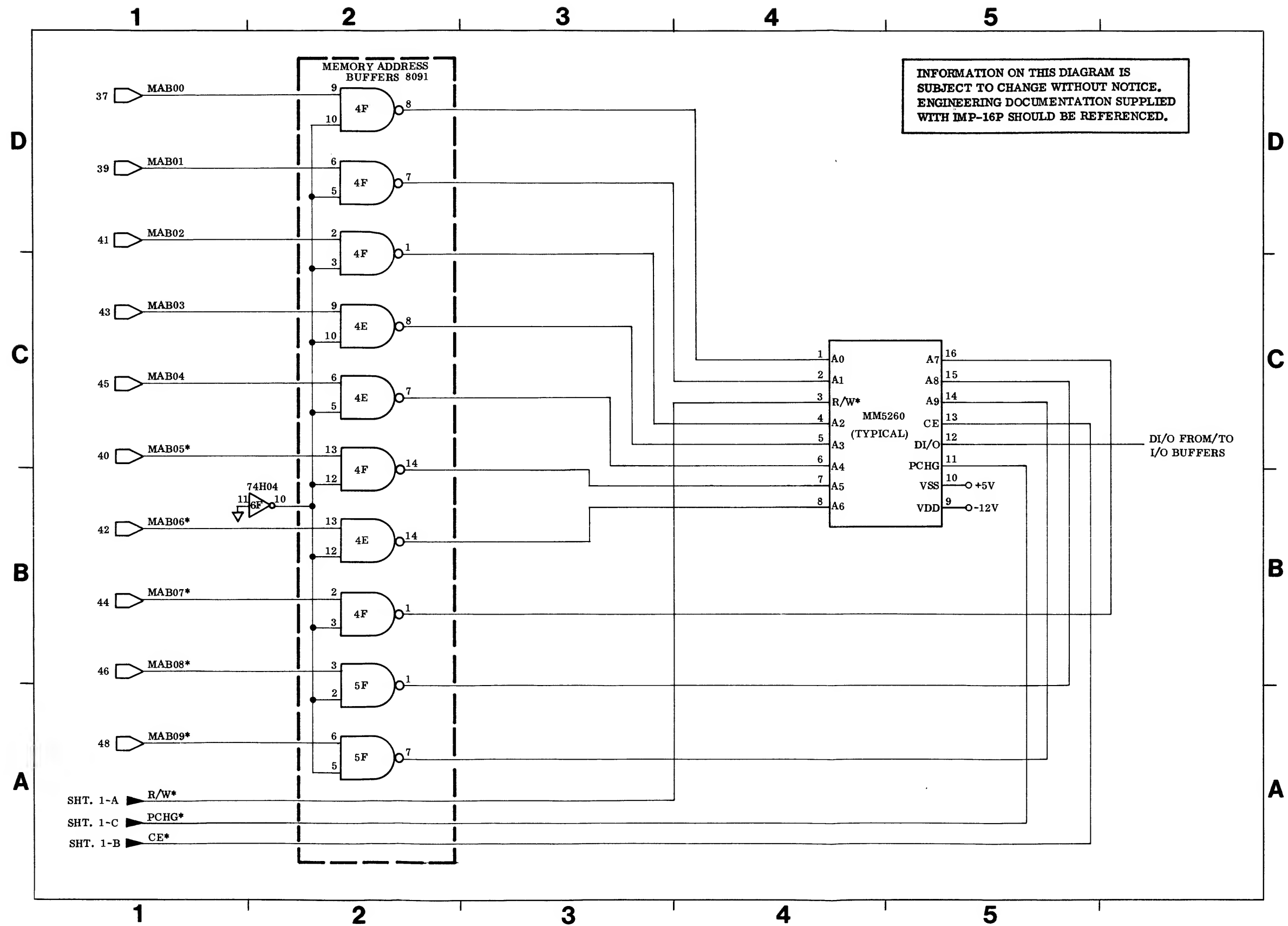
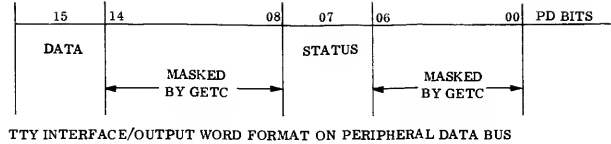
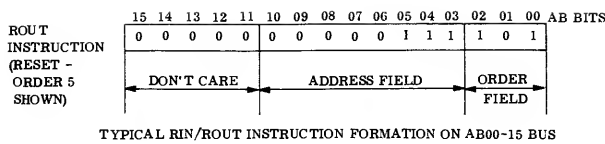
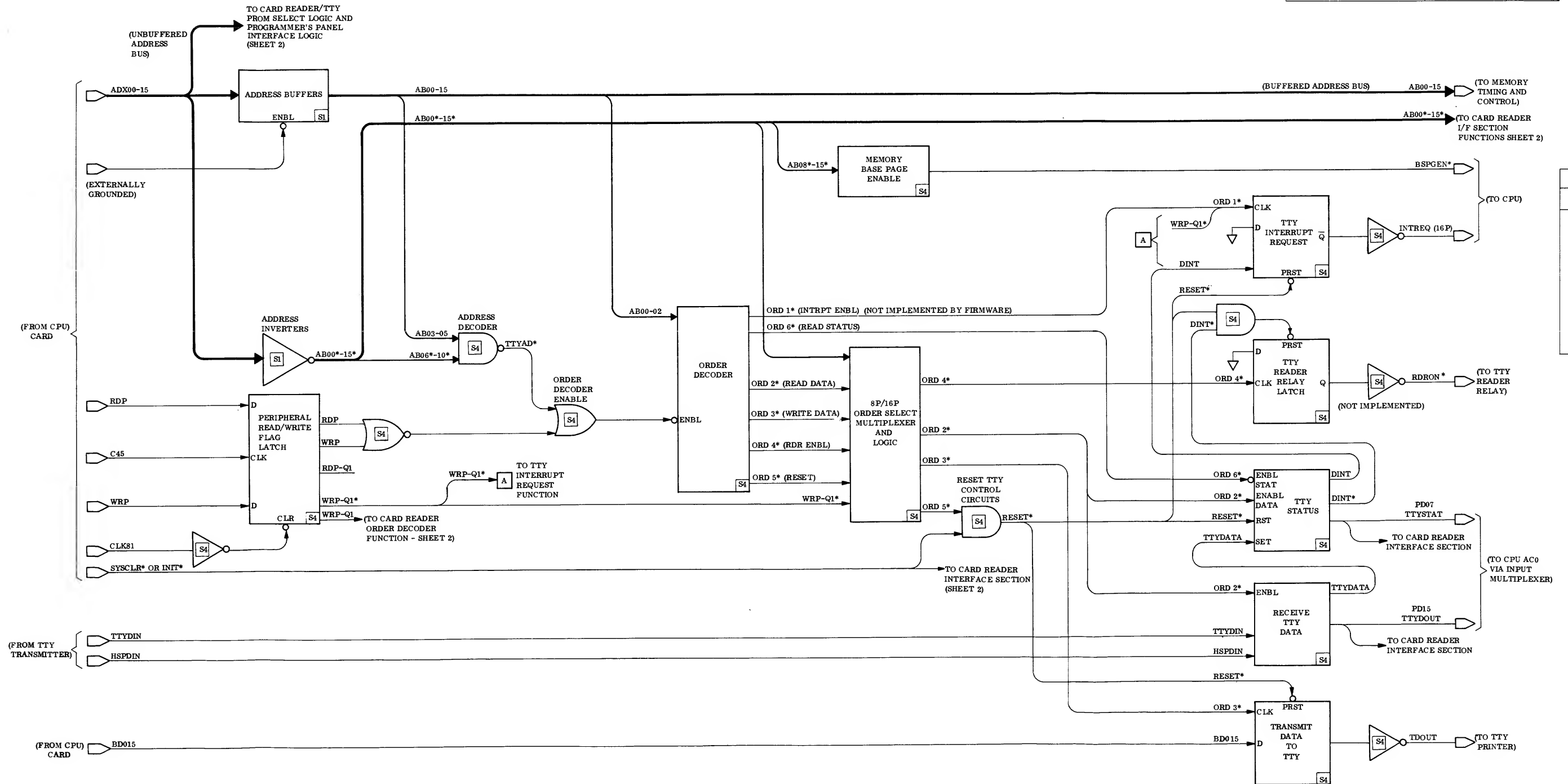


Figure 2/7-7. Memory Storage Card Schematic Diagram (Sheet 3 of 3)
2/7-14

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Function	Output Signal/Logical State (Reset or Initialized)
TTY Interrupt Request	INTREQ/false
TTY Reader Relay Latch	RDRON/false
TTY_Status	TTY_STAT/false DINT/false DINT*/false
Transmit Data to TTY	TDOUT/false



Mnemonic
ABSTT
GETC
PUTC
GECO
SAV
DPLX
MESG
PUT2C
RESET
INTES.
LDM
STM

MINI

Figure 2/7-8.
Func

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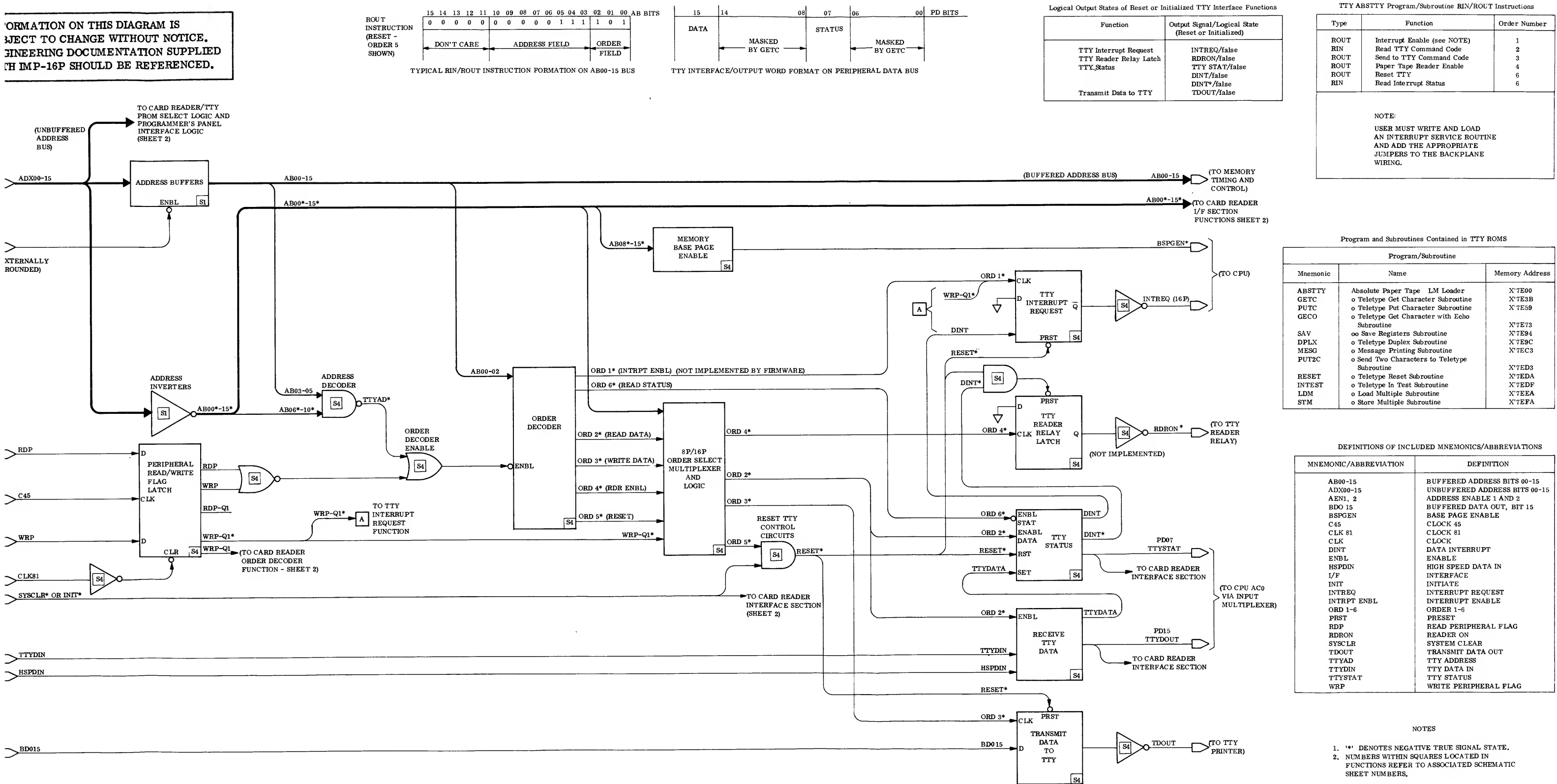
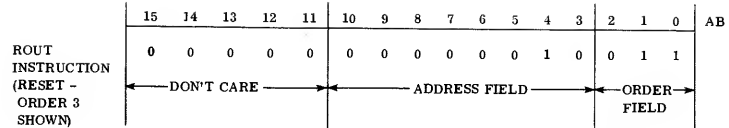
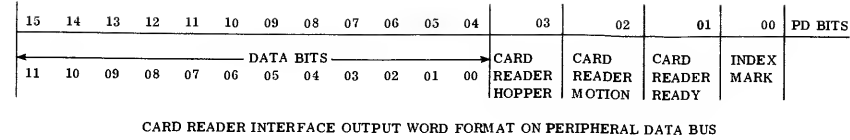
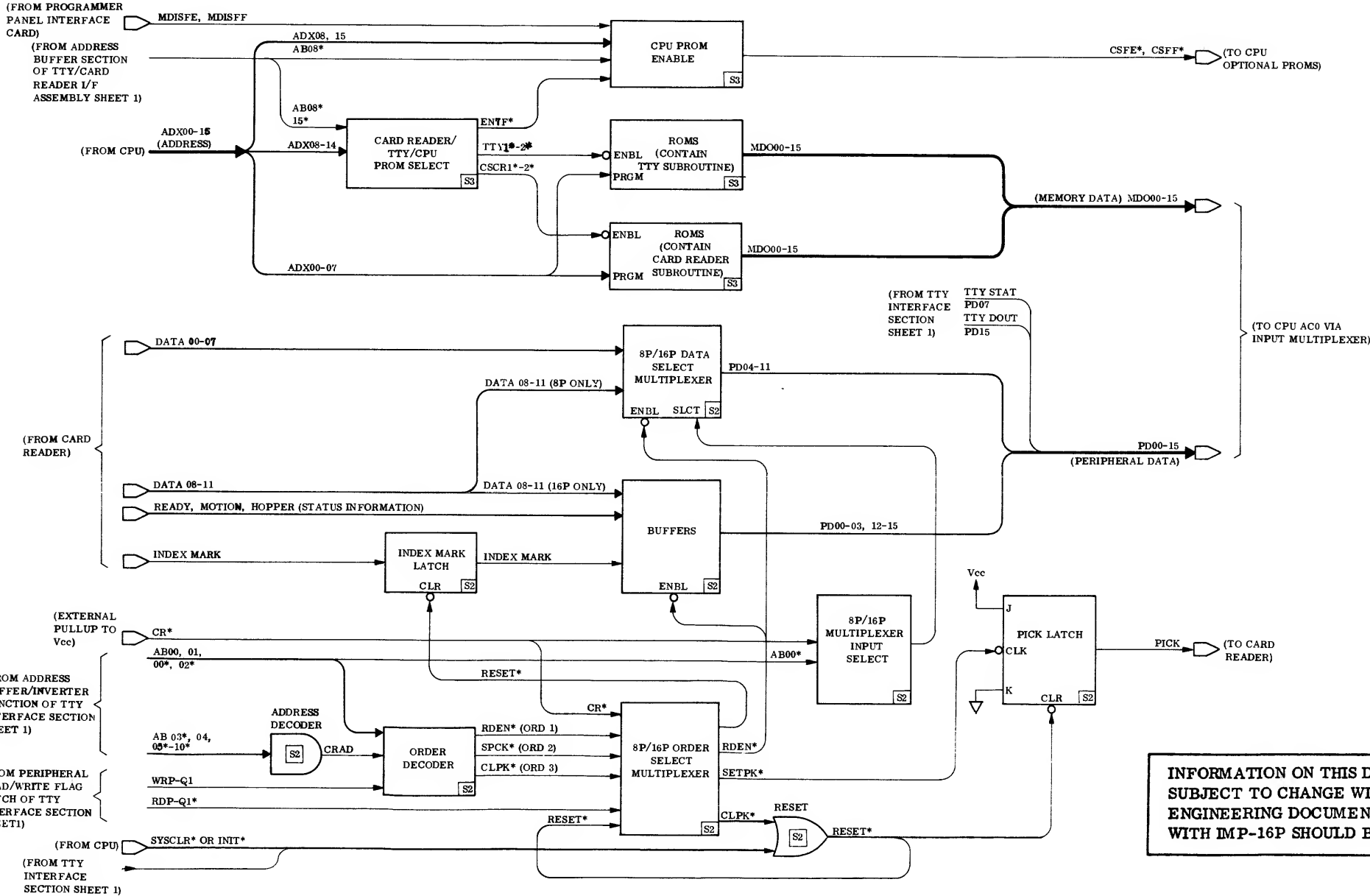


Figure 2/7-8. TTY/Card Reader Interface Card
Functional Block Diagram (Sheet 1 of 2)
2/7-15

INSTRUCTION		
TYPE	FUNCTION	ORDER NUMBER
RIN	READ DATA	1
ROUT	SET PICK	2
ROUT	RESET (INDEX MARK AND PICK LATCH)	3



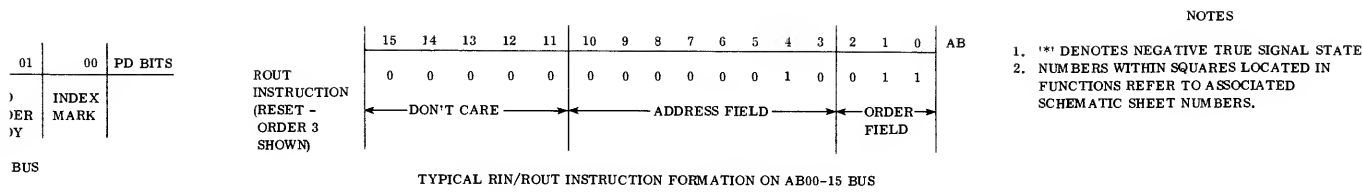
- NOTES
1. '**' DENOTES NEGATIVE TRUE SIGNAL STATE
 2. NUMBERS WITHIN SQUARES LOCATED IN FUNCTIONS REFER TO ASSOCIATED SCHEMATIC SHEET NUMBERS.

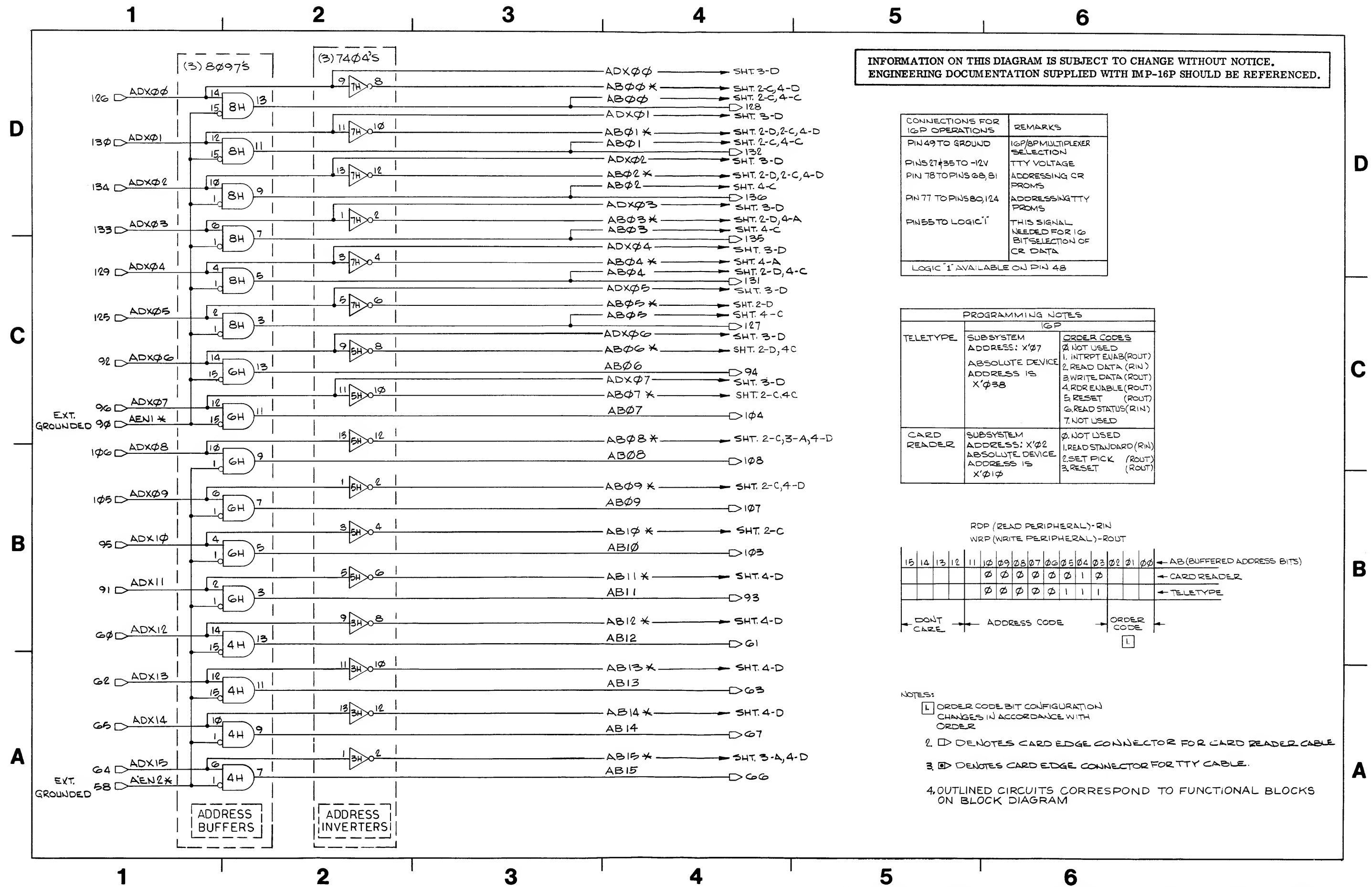


PROGRAMS CONTAINED IN CARD READER PROMS		
MNEMONIC	NAME	MEMORY ADDRESS
ABSCR	ABSOLUTE CARD READER LOADER PROGRAM	X'7F00
RDCOL	• READ AND CONVERT SINGLE COLUMN SUBROUTINE	X'7F2D
CVT	• CONVERT HOLLERITH TO HEX SUBROUTINE	X'7F41
RDWD	• READ AND CONVERT 16-BIT WORD SUBROUTINE	X'7F7F
ENCRD	• END CARD PROCESSING SUBROUTINE	X'7F96
DTCRD	• DATA CARD PROCESSING SUBROUTINE	X'7FA5
RDCRD	• READCARD SUBROUTINE	X'7FD3
CNVRT	• CONVERT BUFFER TO HEX SUBROUTINE	X'7FF4
NOTE		
RDCRD AND CNVRT SUBROUTINES CAN BE IMPLEMENTED BY USER-GENERATED SOFTWARE. THE REMAINING SUBROUTINES ARE IMPLEMENTED BY ABSCR AND ARE NOT INTENDED FOR IMPLEMENTATION BY USER-GENERATED SOFTWARE.		

DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS	
MNEMONIC/ABBREVIATION	DEFINITION
AB00-15	BUFFERED ADDRESS BITS 00-15
ADX00-15	UNBUFFERED ADDRESS BITS 00-15
CLK	CLOCK
CLPK	CLEAR PICK
CLR	CLEAR
CR	CARD READER
CRAD	CARD READER ADDRESS
CSCR1-2	ENABLE CARD READER ROUTINE, PROMS 1 AND 2
EN7F	ENABLE PAGE 7F
ENBL	ENABLE
INIT	INITIATE
MDISFE, FF	MEMORY DISABLE, PAGE FE AND FF
MDO00-15	MEMORY DATA BITS 00-15
PD00-15	PERIPHERAL DATA BITS 00-15
PRGM	PROGRAM
RDEN	READ ENABLE
SLCT	SELECT
SPCK	SET PICK
SYSLR	SYSTEM CLEAR
TTY 1-2	ENABLE TELETYPE ROUTINE, PROMS 1 AND 2
WRP	WRITE PERIPHERAL

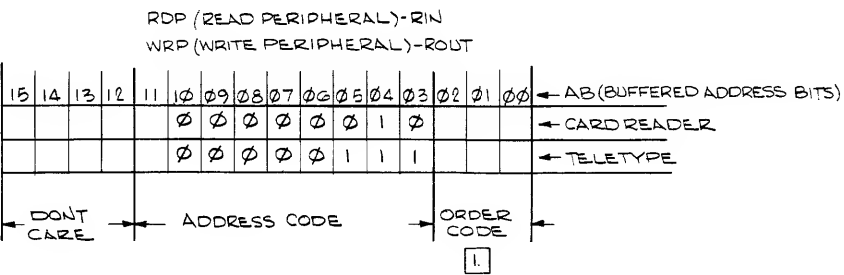
Figure 2/7-8.
Func





CONNECTIONS FOR IGP OPERATIONS	REMARKS
PIN 49 TO GROUND	IGP/SP MULTIPLEXER SELECTION
PINS 27 & 35 TO -12V	TTY VOLTAGE
PIN 78 TO PINS 68, 81	ADDRESSING CR PROMS
PIN 77 TO PINS 80, 124	ADDRESSING TTY PROMS
PIN 55 TO LOGIC "1"	THIS SIGNAL NEEDED FOR IGP BIT SELECTION OF CR DATA
LOGIC "1" AVAILABLE ON PIN 48	

PROGRAMMING NOTES		
IGP		
TELETYPE	SUBSYSTEM ADDRESS: X'07 ABSOLUTE DEVICE ADDRESS IS X'038	ORDER CODES 0. NOT USED 1. INTRPT ENAB (ROUT) 2. READ DATA (RIN) 3. WRITE DATA (ROUT) 4. RDRE ENAB (ROUT) 5. RESET (ROUT) 6. READ STATUS (RIN) 7. NOT USED
CARD READER	SUBSYSTEM ADDRESS: X'02 ABSOLUTE DEVICE ADDRESS IS X'010	0. NOT USED 1. READ STANDARD (RIN) 2. SET PICK (ROUT) 3. RESET (ROUT)



- NOTES:
- 1. ORDER CODE BIT CONFIGURATION CHANGES IN ACCORDANCE WITH ORDER
 - 2. □ DENOTES CARD EDGE CONNECTOR FOR CARD READER CABLE
 - 3. □ DENOTES CARD EDGE CONNECTOR FOR TTY CABLE
 - 4. OUTLINED CIRCUITS CORRESPOND TO FUNCTIONAL BLOCKS ON BLOCK DIAGRAM

Figure 2/7-9. TTY/Card Reader Interface Card Schematic Diagram (Sheet 1 of 4)
2/7-17

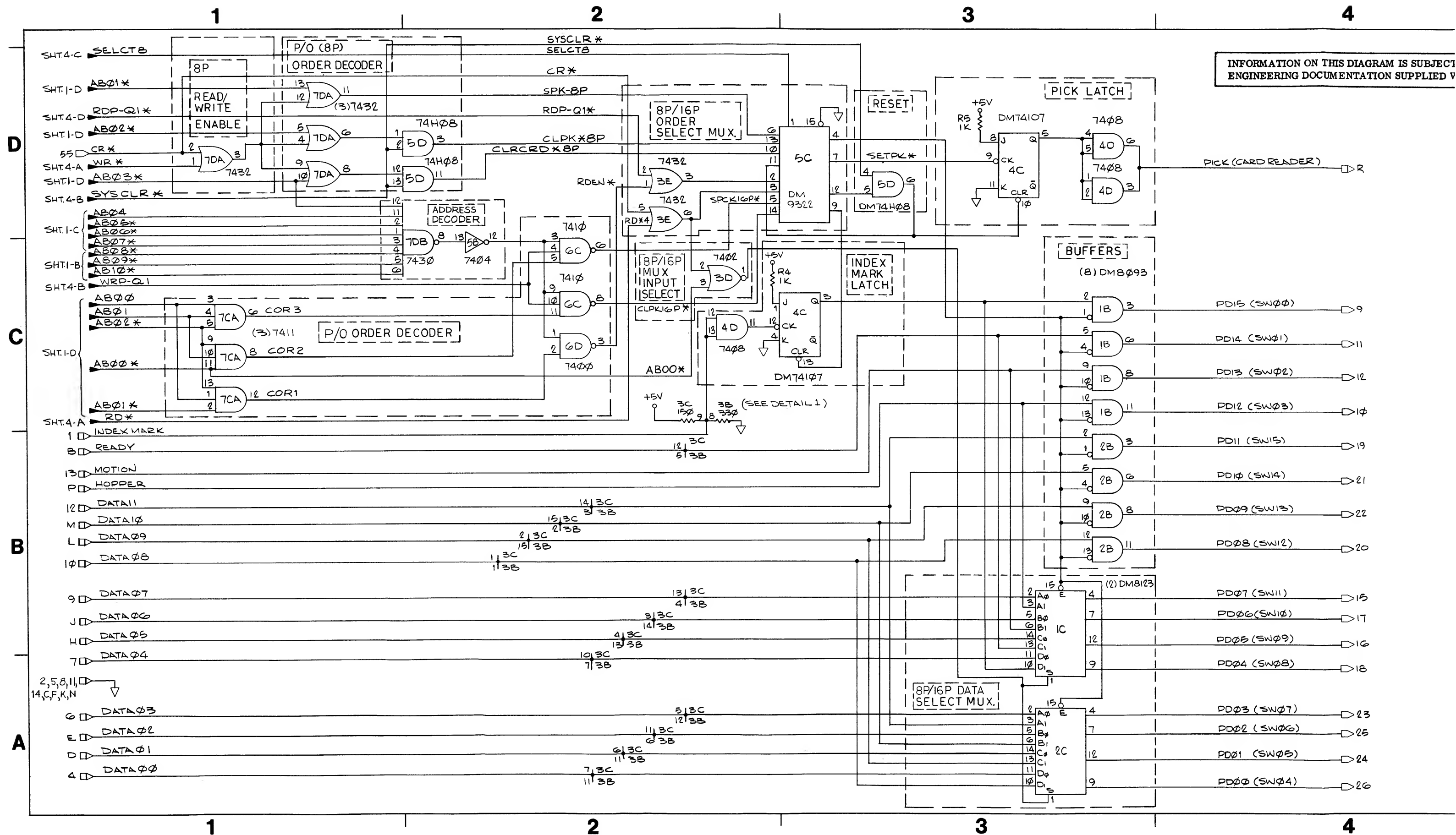


Figure 2/7-9.

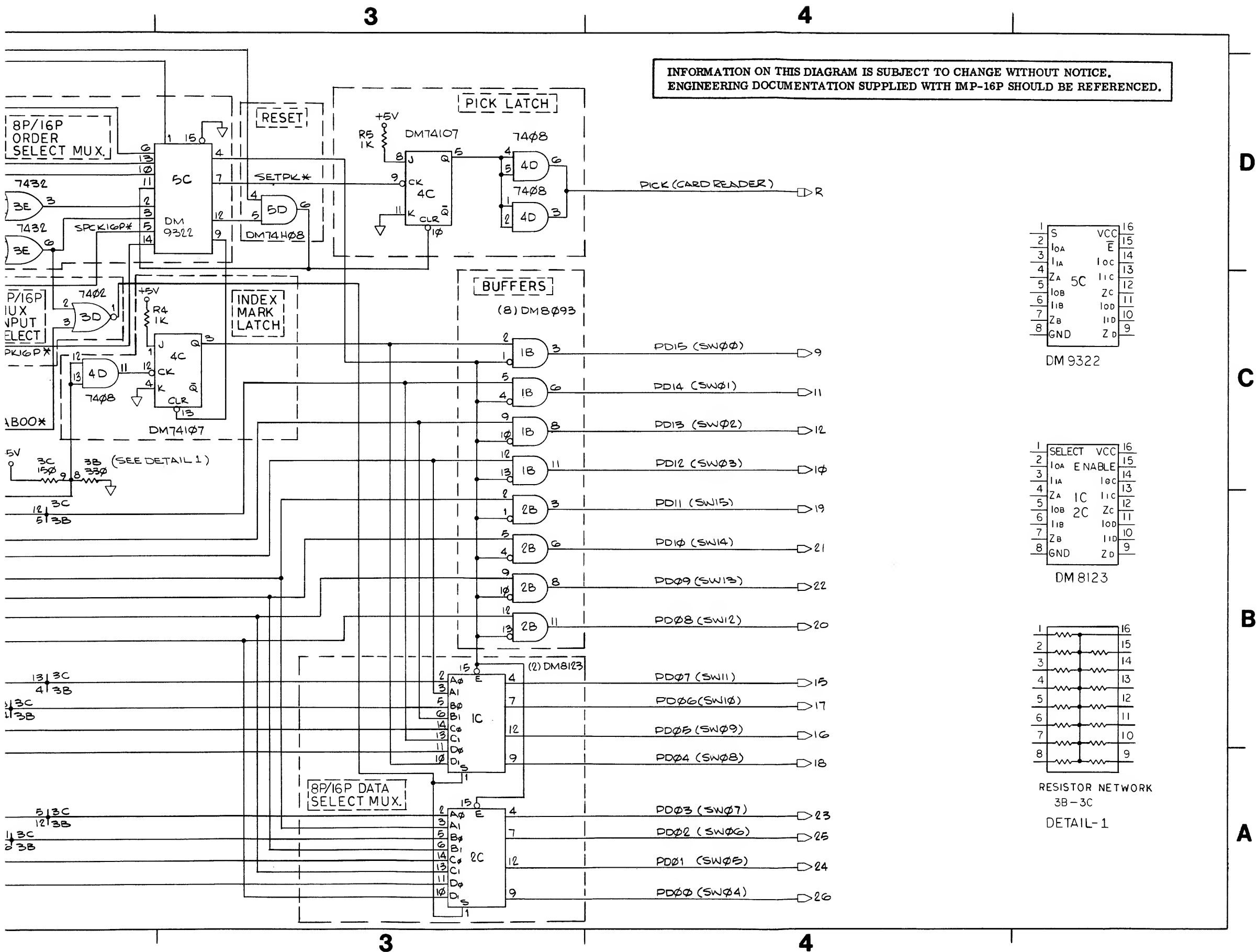


Figure 2/7-9. TTY/Card Reader Interface Card
 Schematic Diagram (Sheet 2 of 4)
 2/7-18

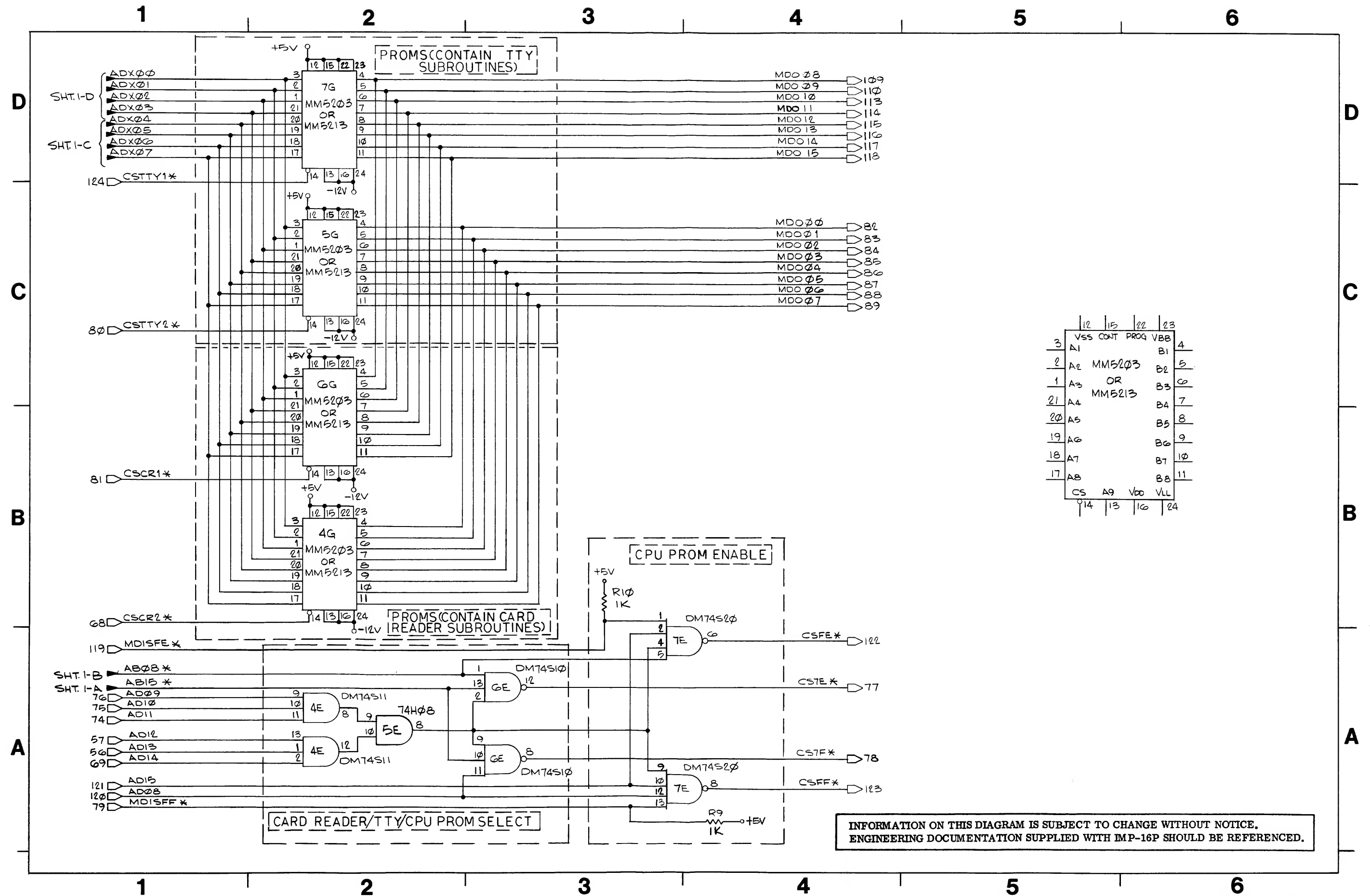
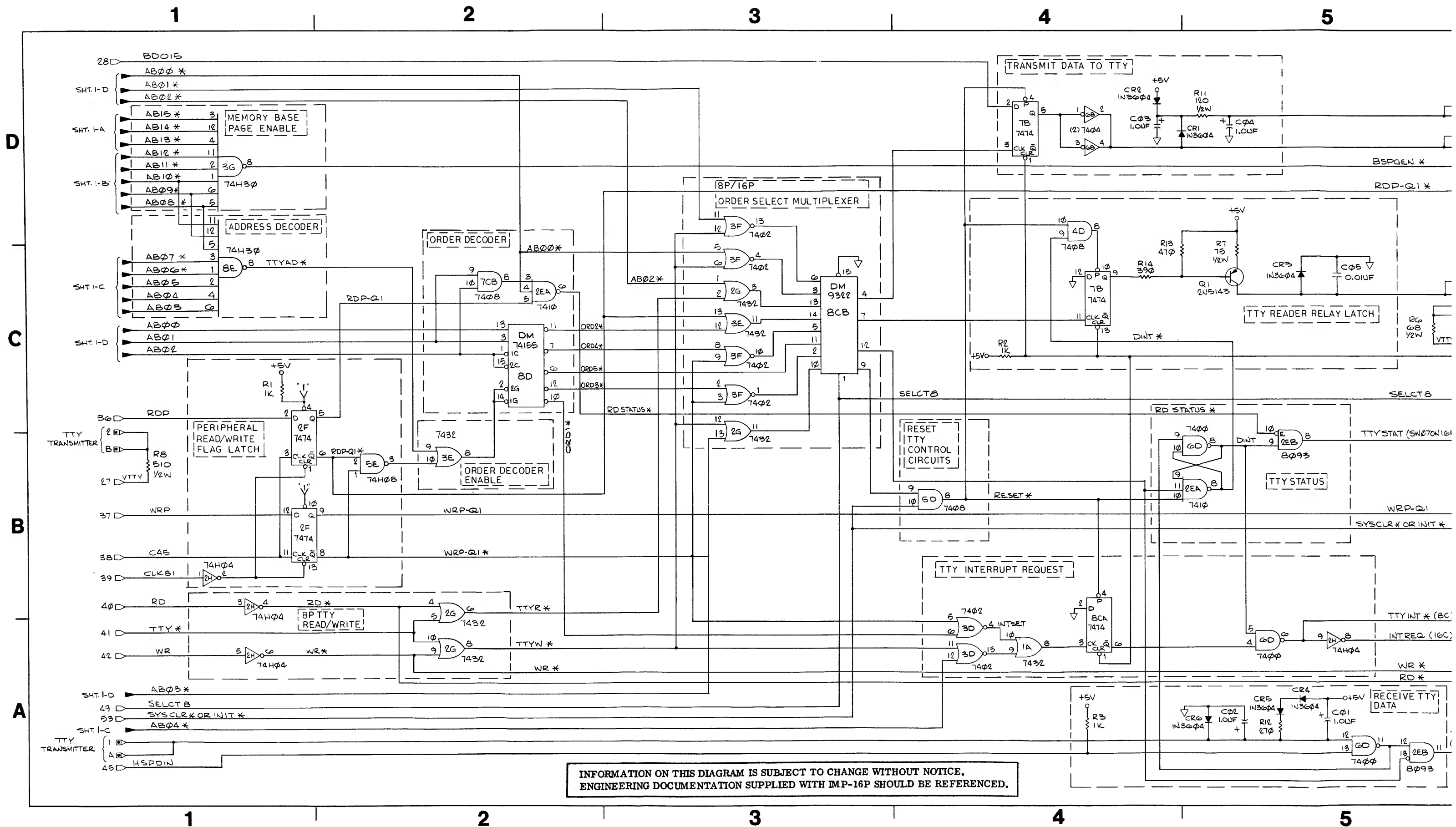


Figure 2/7-9. TTY/Card Reader Interface Card Schematic Diagram (Sheet 3 of 4)
2/7-19



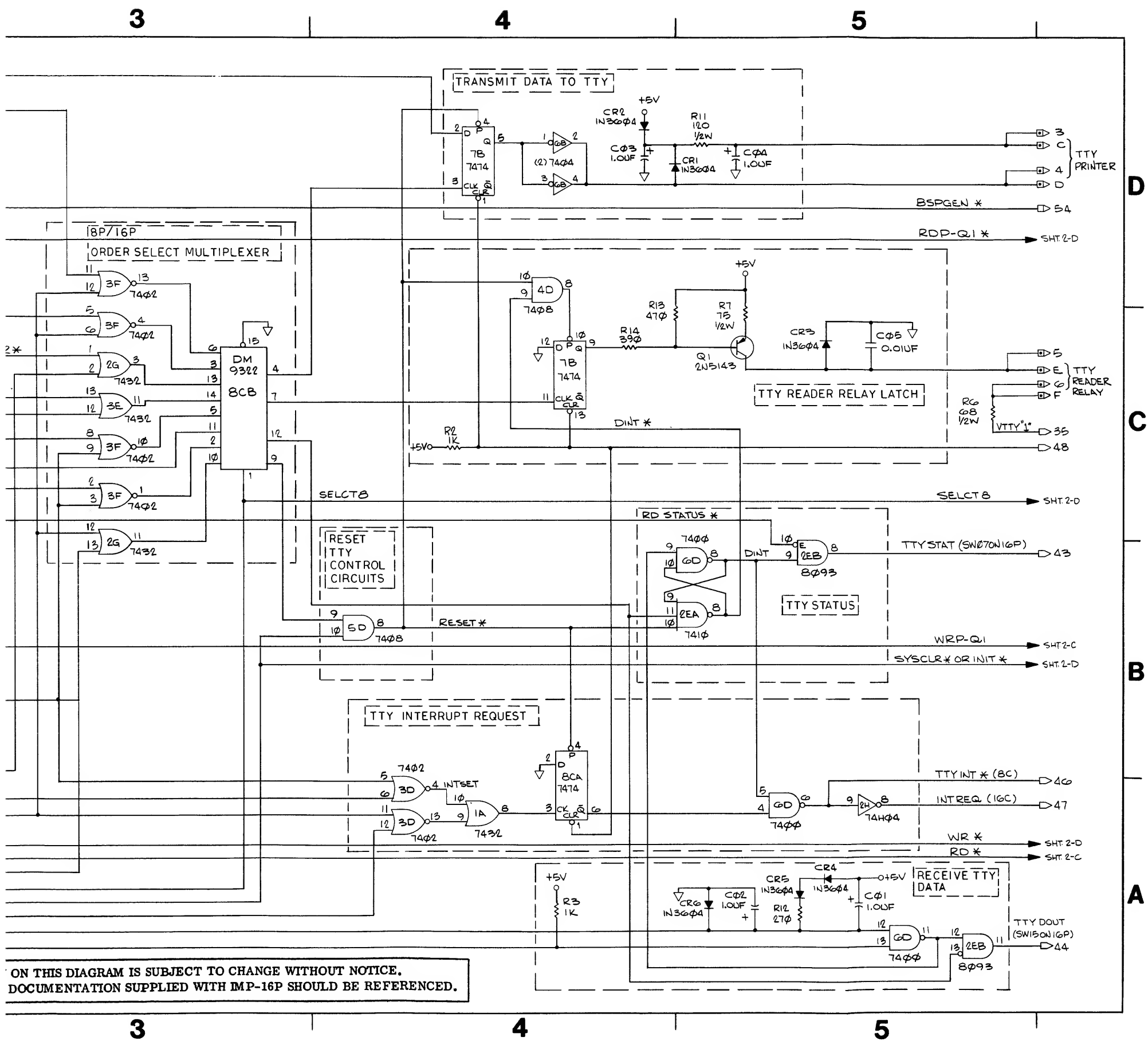


Figure 2/7-9. TTY/Card Reader Interface Card
Schematic Diagram (Sheet 4 of 4)
2/7-20

Figure 2/7-10. Programmers Panel Card Schematic Diagram (Sheet 1 of 2)

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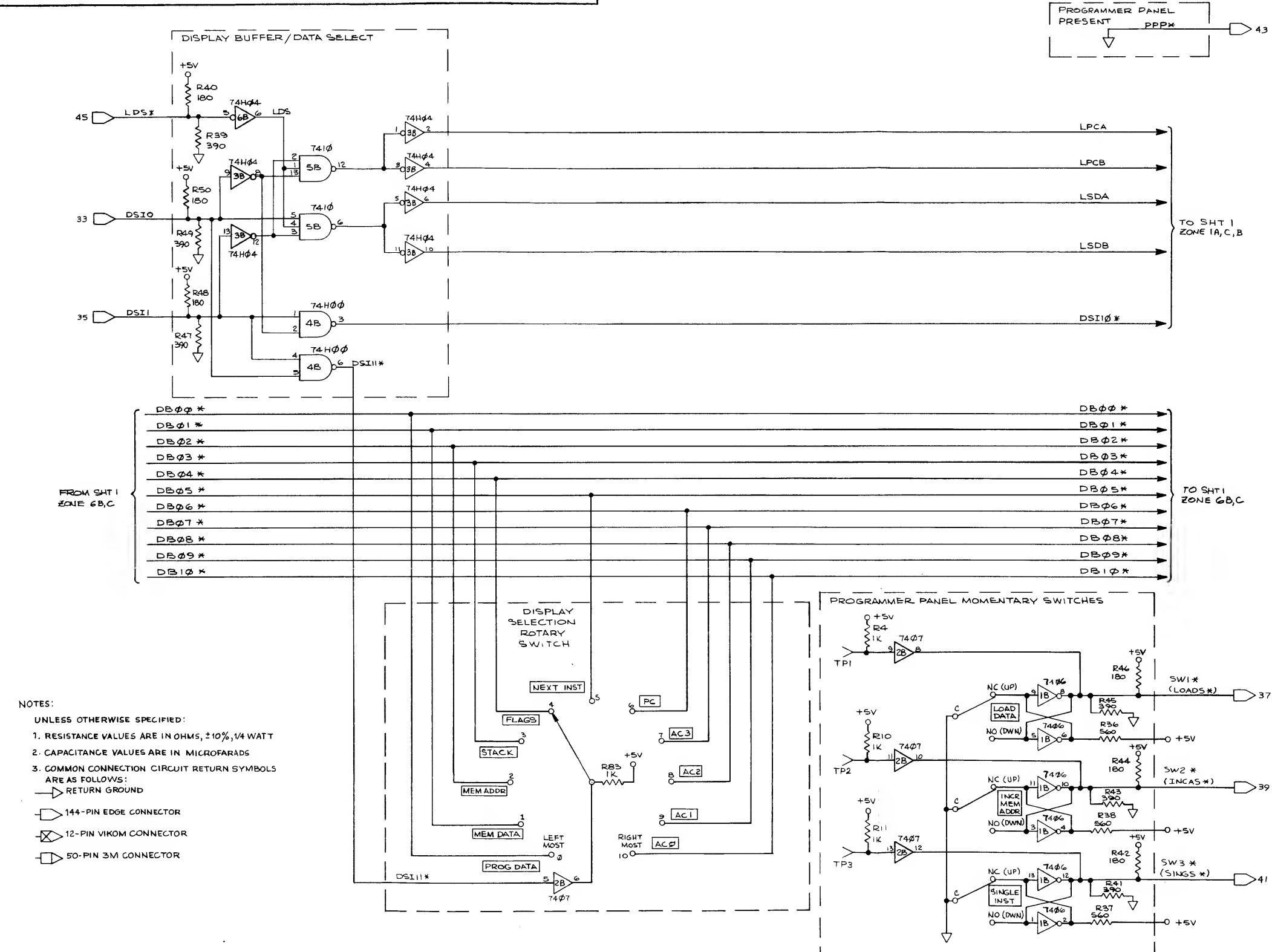


Figure 2/7-10. Programmers Panel Card Schematic Diagram (Sheet 2 of 2)

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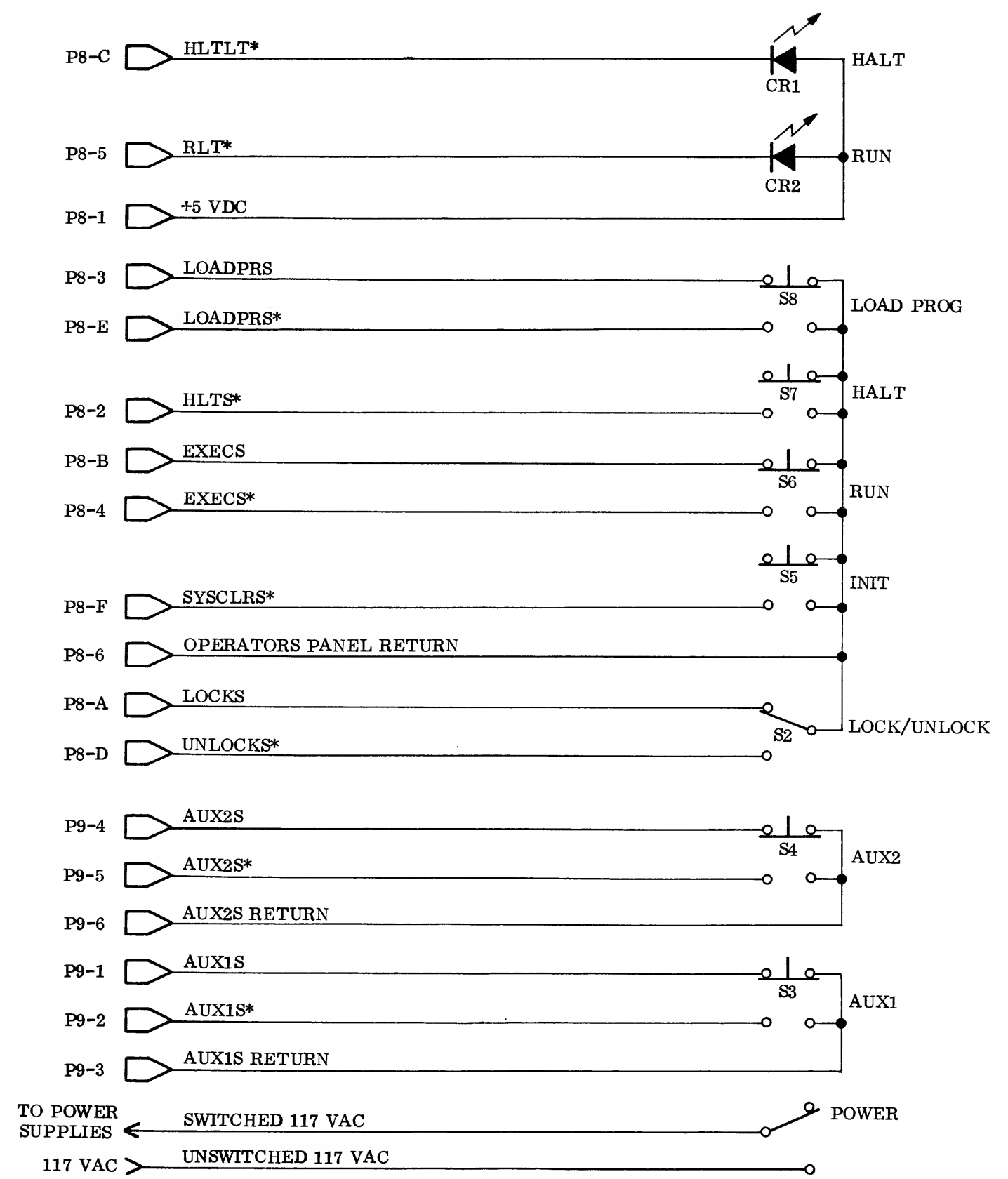


Figure 2/7-11. Operators Control Panel Schematic Diagram
2/7-23

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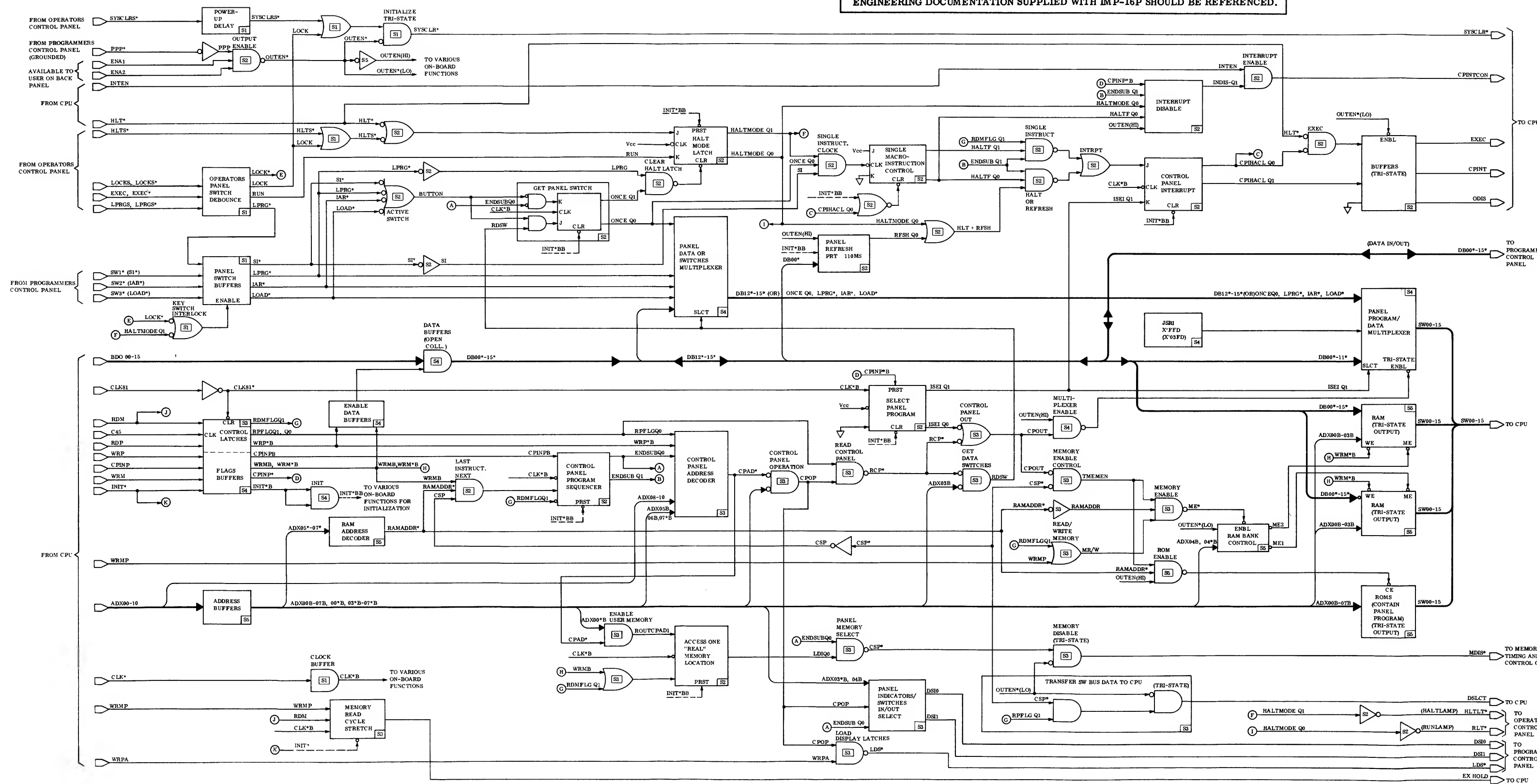
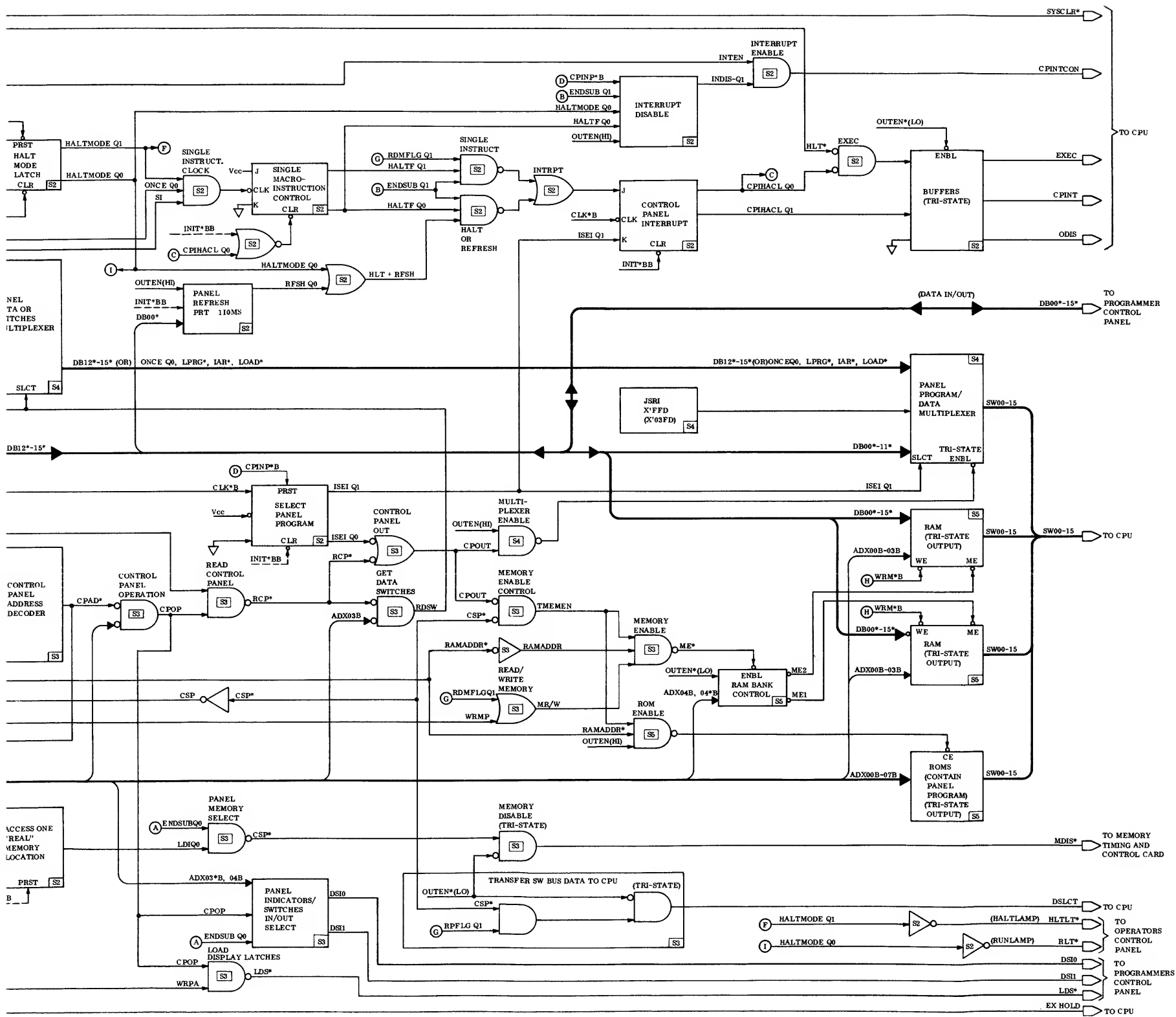


Figure 2/7-12

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DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS	
MNEMONIC/ABBREVIATION	DEFINITION
ADX 00-10	ADDRESS BITS 00-10
BDO 00-15	BUFFERED DATA OUT BITS 00-15
C45	CLOCK 45
CLK	CLOCK
CLK 81	CLOCK 81
CLK*B	CLOCK*BUFFERED
CLR	CLEAR
CPAD	CONTROL PANEL ADDRESS
CPHACL	CONTROL PANEL INTERRUPT HALT CONTROL
CPINP	CONTROL PANEL INPUT
CPINPB	CONTROL PANEL INPUT BUFFERED
CPINT	CONTROL PANEL INTERRUPT
CPINT CON	CONTROL PANEL INTERRUPT CONTROL
CPOP	CONTROL PANEL OPERATION
CPOUT	CONTROL PANEL OUTPUT
CSP	CHIP SELECT PANEL
DB 00-15	DATA BITS 00-15
DSI 0, 1	DATA SWITCH/INDICATORS 0, 1
ENA 1, 2	ENABLE 1, 2
END SUB	END OF SUBROUTINE (PANEL)
EXEC	EXECUTE
EX HOLD	EXTRA HOLD (CLOCK 4)
HLT	HALT
HLT + RF5H	HALT OR REFRESH
HLT LT	HALT LIGHT
HLTS	HALT SWITCH
IAR	INCREMENT ADDRESS REGISTER
INT	INITIATE
INIT*BB	INITIATE* BUFFERED TWICE
INTEN	INTERRUPT ENABLE
LDI	LOAD IMMEDIATE
LDS	LOAD DISPLAY LATCHES
LOCKS	LOCK SWITCH
LPRG	LOAD PROGRAM
LPRGS	LOAD PROGRAM SWITCH
MDIS	MEMORY DISABLE
ME 1, 2	MEMORY ENABLE 1, 2
MR/W	MEMORY READ/WRITE
ODIS	OUTPUT DISABLE
OUTEN	OUTPUT ENABLE
PPP	PROGRAMMER PANEL CARD IN PLACE
PRST	PRESET
RAMADDR	RAM ADDRESS
RCP	READ CONTROL PANEL
RDM	READ MEMORY
RDMFLG	READ MEMORY FLAG
RDSW	READ SWITCHES
ROUT CPAD 1	REGISTER OUT, CONTROL PANEL ADDRESS, 1
RPFLG	READ PERIPHERAL FLAG
RF5H	REFRESH
SI	SINGLE INSTRUCTION
SLCT	SELECT
SW 00-15	SWITCHED BITS 00-15
SW 1, 2, 3	SWITCH 1, 2, 3
SYSCLS	SYSTEM CLEAR SWITCH
TMEMEN	TRANSPARENT MEMORY ENABLE
WRM	WRITE MEMORY
WRMB	WRITE MEMORY BUFFERED
WRMP	WRITE MEMORY PERIPHERAL
WRPA	WRITE PERIPHERAL A

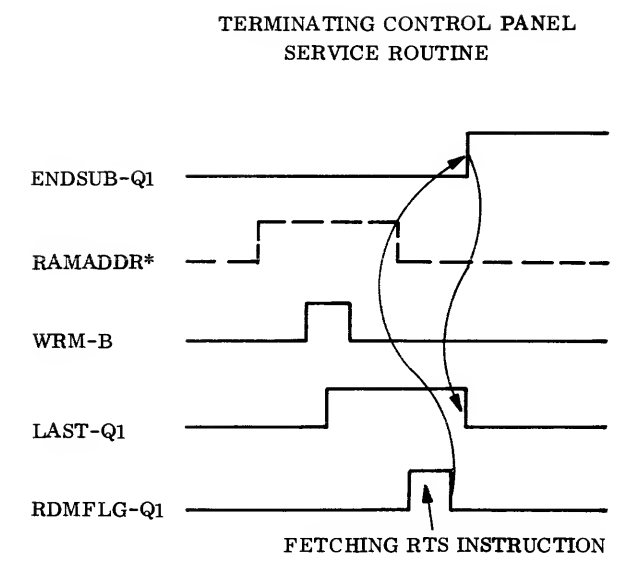
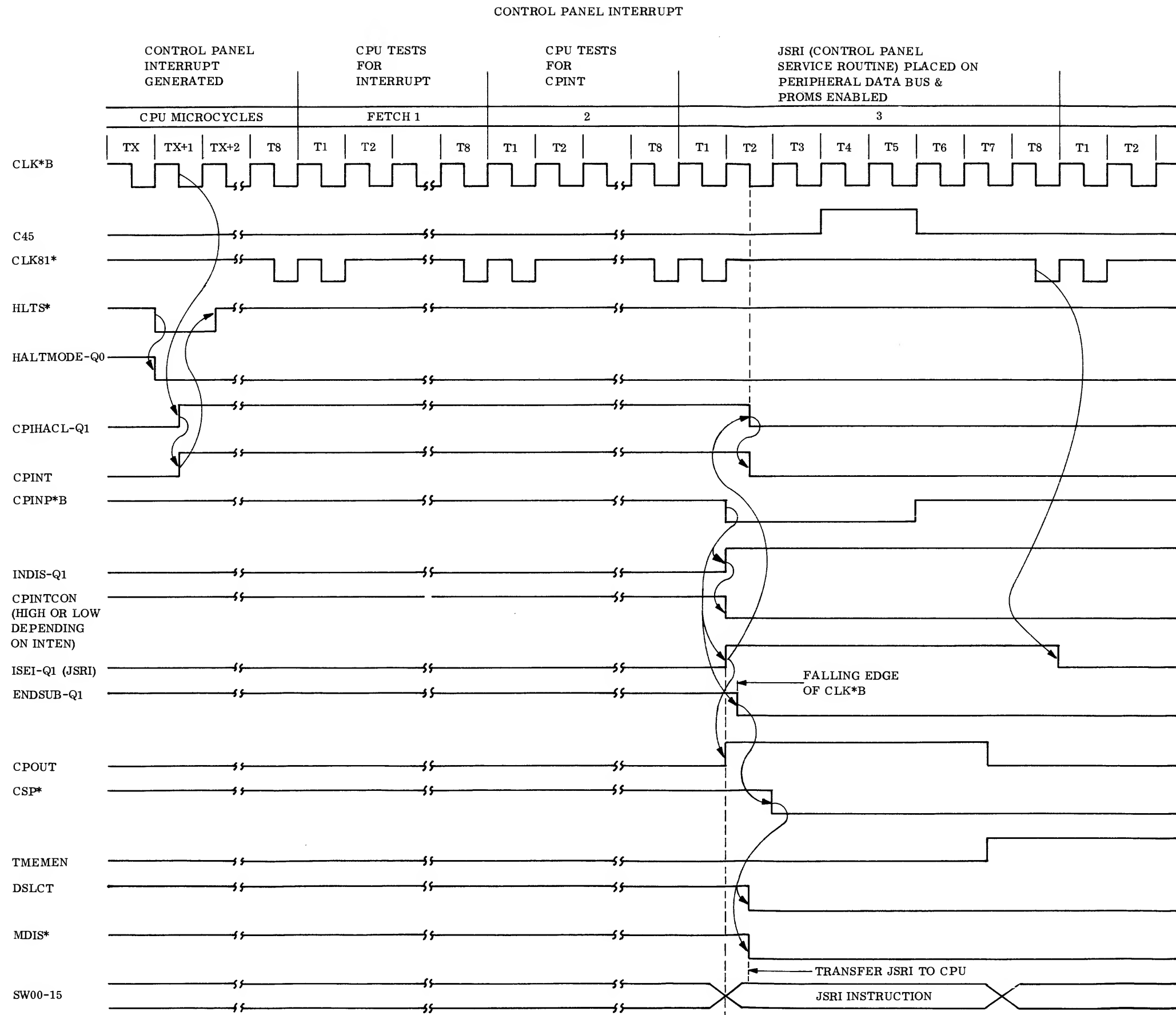
1. '*' DENOTES NEGATIVE TRUE SIGNAL STATE
2. NUMBERS PRECEDED BY 'S'
WITHIN FUNCTIONAL BLOCKS
DENOTE ASSOCIATED SCHEMATIC
SHEET NUMBERS.

DS10	DS1	OPERATION
LOW	LOW	WRITE DATA INTO PROGRAM COUNTER/MEMORY ADDRESS LATCHES WHEN LDS* TRUE
LOW	HIGH	READ STATUS OF DATA SWITCHES
HIGH	LOW	WRITE DATA INTO DATA DISPLAY LATCHES WHEN LDS* IS TRUE
HIGH	HIGH	READ DISPLAY SELECTOR SWITCH POSITION

Control Panel Service Routine RIN/ROUT Instructions			
INSTRUCTION			
Type	Function	Mnemonic	Control Field Value
RIN	Get Control Panel Command Switches	GPCS	X'18
RIN	Get Control Panel Data Switches	GDS	X'10
ROUT	Load Control Panel Program Counter Display Register	LPCDR	X'00
ROUT	Load Control Panel Data Register	LDR	X'08
ROUT	Enable User Memory	EUM	X'01

Transparent Memory Locations of Saved CPU Contents	
Transparent Memory Location (Hexadecimal)	CPU Contents
FF01	AC0
FF02	AC1
FF03	AC2
FF04	AC3
FF05	Program Counter (current top-of-stack). Displayed PC.
FF06	Previous top-of-stack. Stack display word.
FF07-FF14	Stack 1 through stack 14, respectively
FF15	Displayed flags
FF16	RALU flags
FF17	Memory Address Pointer
FF18-FF1F	Scratch pad (unused)

Figure 2/7-12. Control Panel Interface Card
Functional Block Diagram
2/7-24



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Figure 2/7-13. Control Panel Interface Card Timing Diagram (Sheet 1 of 2)
2/7-25

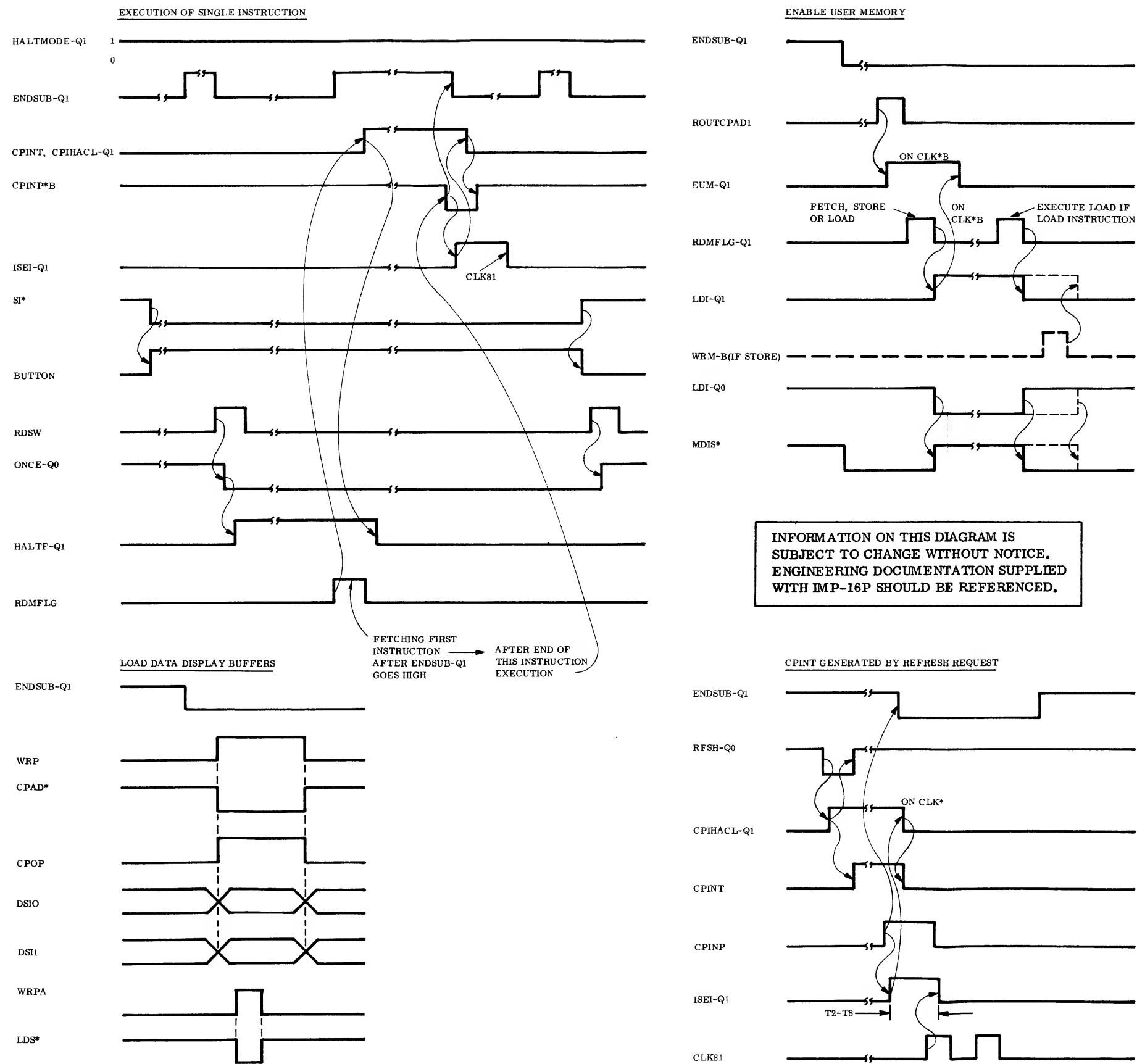
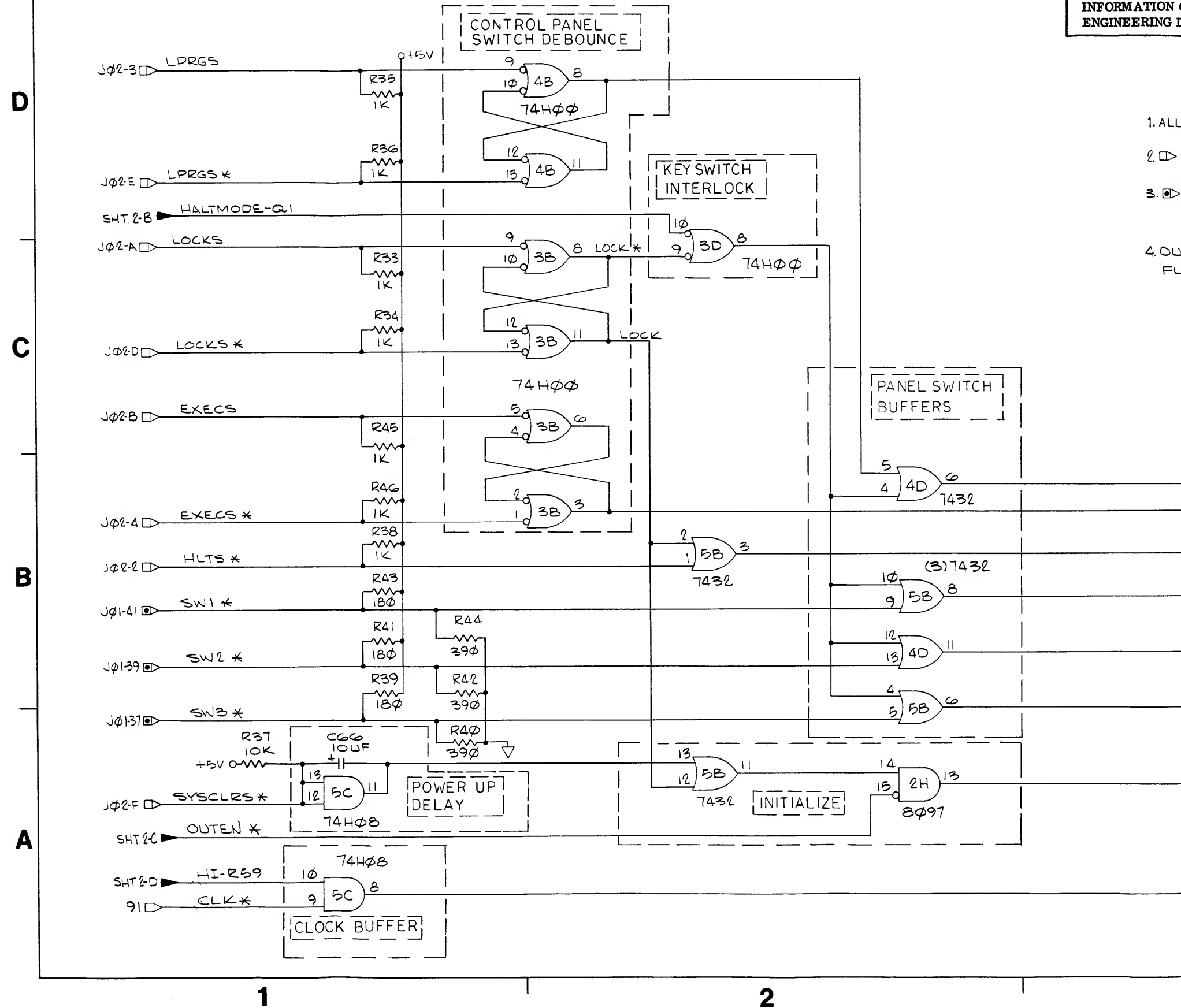
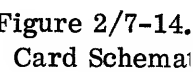
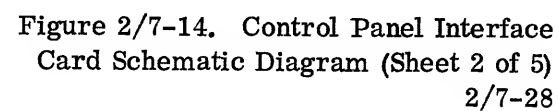
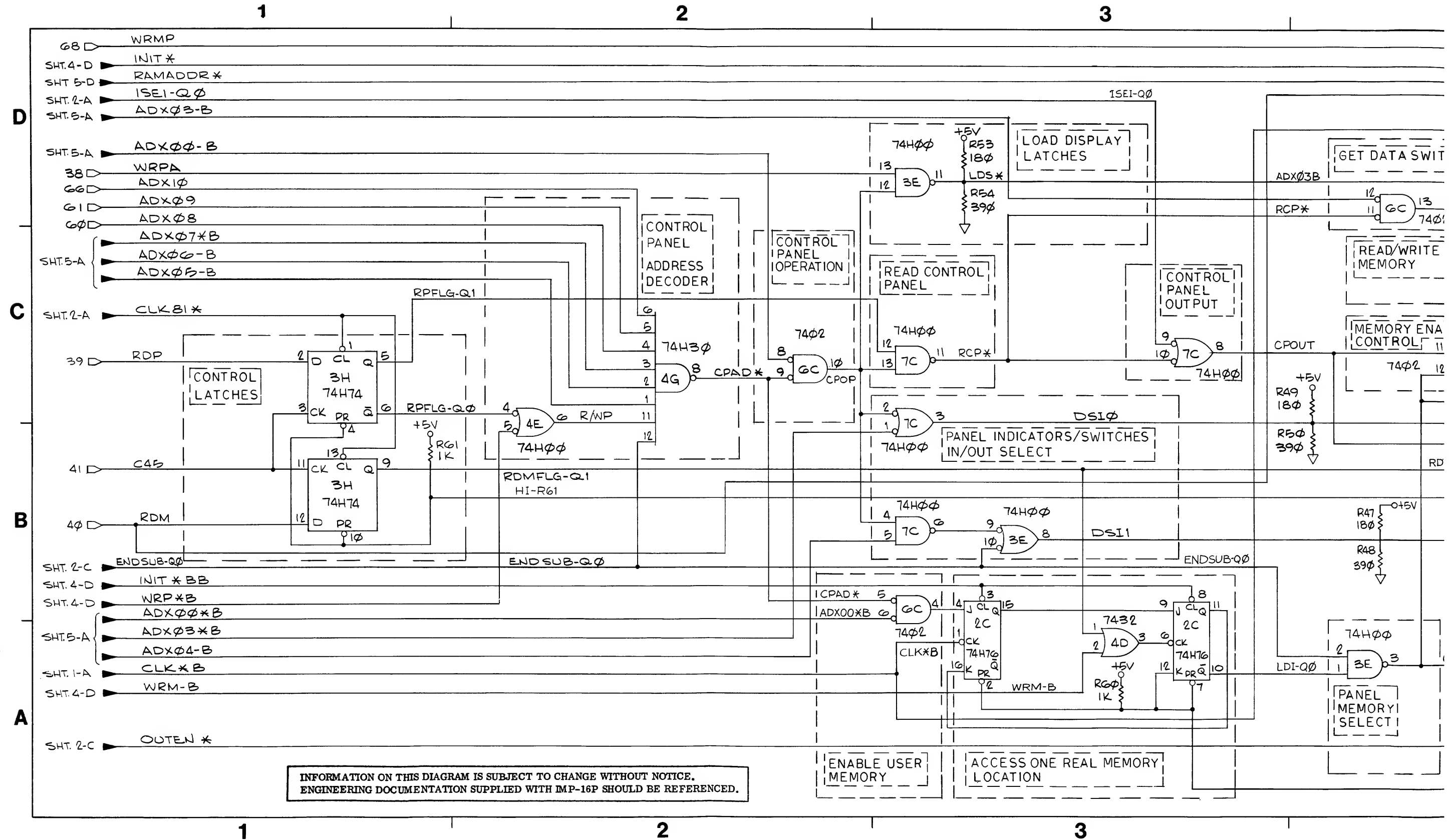


Figure 2/7-13. Control Panel Interface Card Timing Diagram (Sheet 2 of 2)
2/7-26









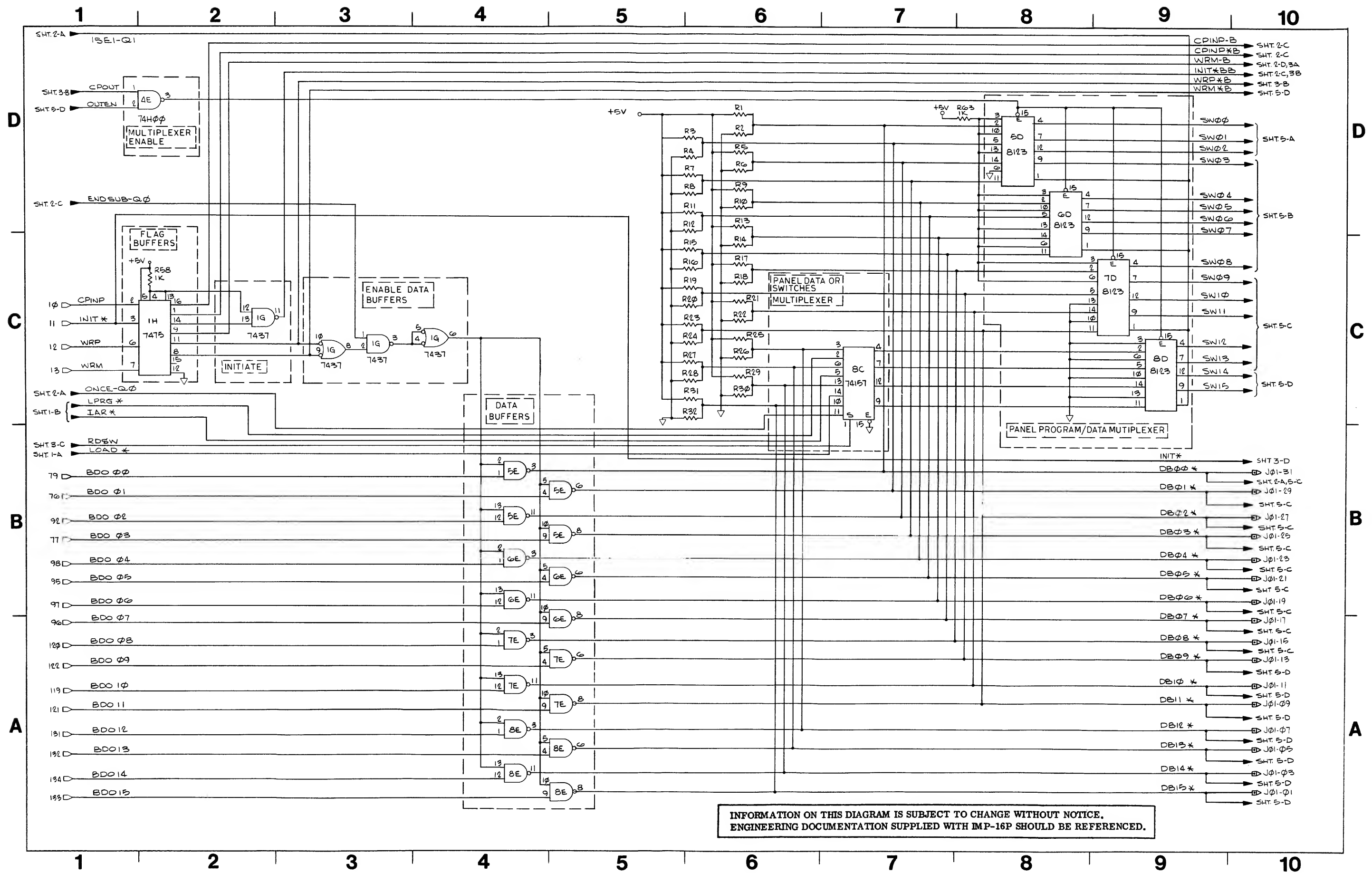


Figure 2/7-14

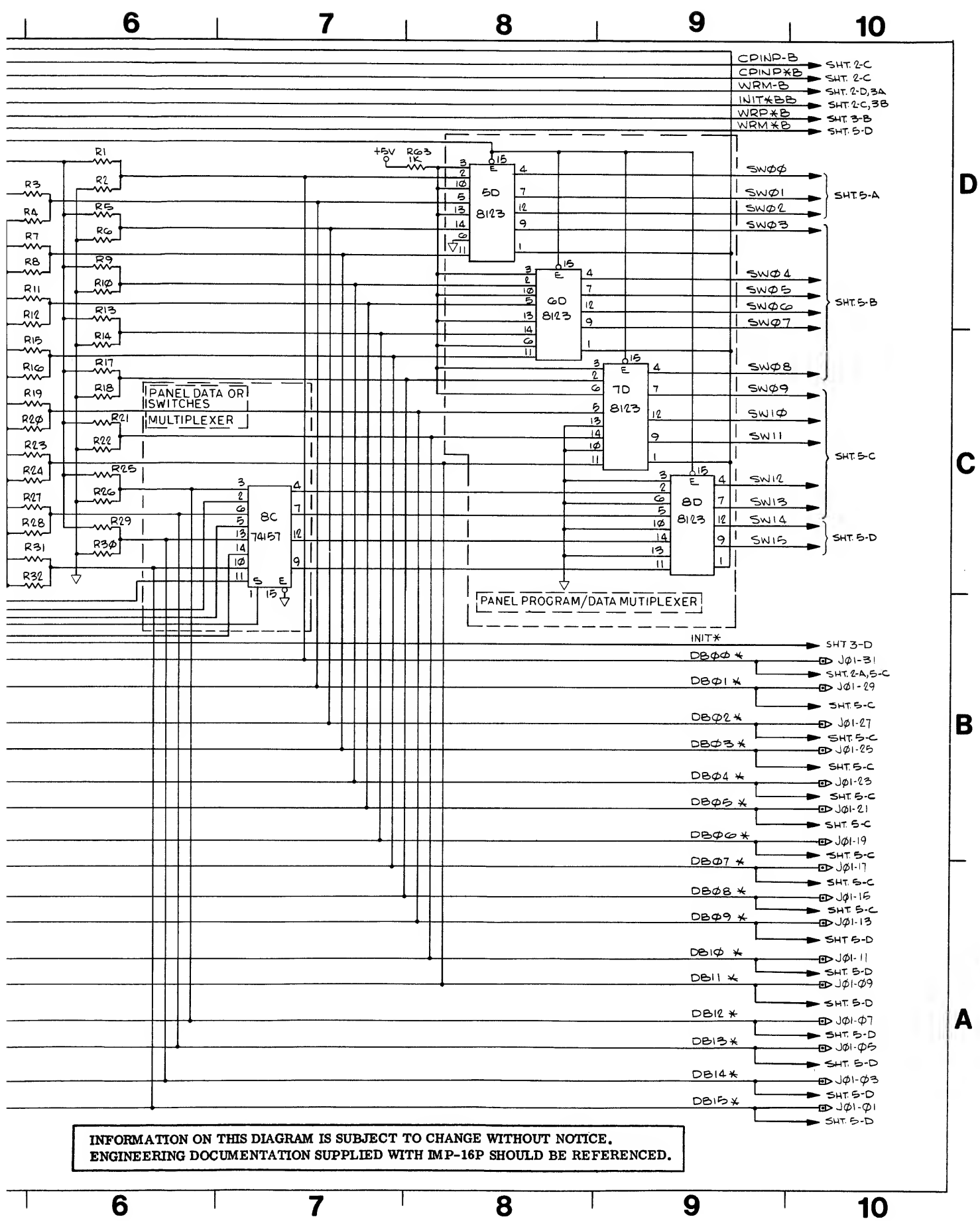
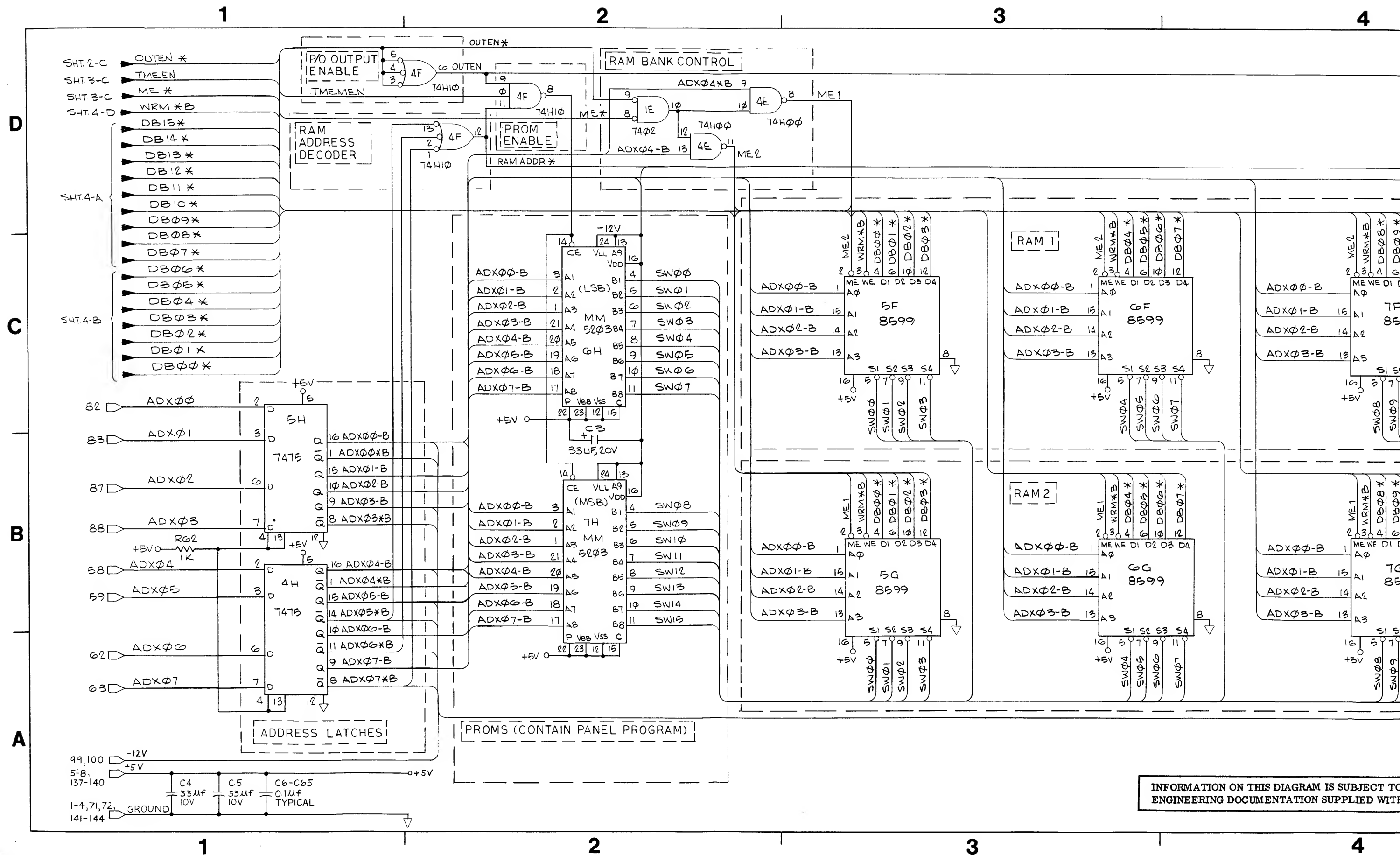
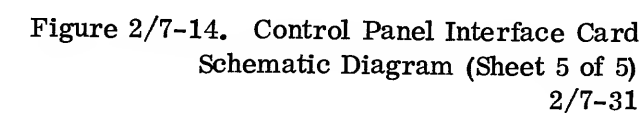


Figure 2/7-14. Control Panel Interface Card Schematic Diagram (Sheet 4 of 5)
 2/7-30





Appendix A
LIST OF MNEMONICS/ABBREVIATIONS

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources

Mnemonic/ Abbreviation	Definition	Source/Reference
A0-A9	Memory Chip Row Address Bits 0-9	Memory Storage Card
AB00-15	Buffered Address Bits 00-15	TTY/Card Reader Interface Card
ABSCR	Absolute Card Reader Loader Routine	In ROM on TTY/Card Reader Interface Card
ABSTTY	Absolute Paper Tape LM Loader Routine	In ROM on TTY/Card Reader Interface Card
ADLCHLD	Address Latch Load	Memory Timing and Control Card
ADX00-15	Unbuffered Address Bits 00-15	CPU Card
AEN1, 2	Address Enable 1, 2	TTY/Card Reader Interface Card
AUX1, 2	Auxiliary Switches 1, 2	Operators Control Panel
BDO00-15	Buffered Data Out Bits 00-15	CPU Card
BSPGEN	Base Page Enable	TTY/Card Reader Interface Card
C45	Clock 45	CPU Card
CE	Chip Enable	Memory Storage Card
CI	Cycle Initiate	Memory Timing and Control Card
CLK	Clock	- -
CLK81	Clock 81	CPU Card
CLK*B	Clock * Buffered	Control Panel Interface Card
CLKENBL	Clock Enable	Memory Timing and Control Card
CLMCTL	Column Control	Memory Timing and Control Card
CLPK	Clear Pick	TTY/Card Reader Interface Card
CLR	Clear	- -
CNVRT	Convert Buffer to Hex Subroutine	In ROM on TTY/Card Reader Interface Card
CPAD	Control Panel Address	Control Panel Interface Card
CPIHACL	Control Panel Interrupt Halt Control	Control Panel Interface Card
CPINP	Control Panel Input	CPU Card
CPINPB	Control Panel Input Buffered	Control Panel Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
CPINT	Control Panel Interrupt	Control Panel Interface Card
CPINTCON	Control Panel Interrupt Control	Control Panel Interface Card
CPOP	Control Panel Operation	Control Panel Interface Card
CPOUT	Control Panel Output	Control Panel Interface Card
CR	Cycle Request	CPU Card
CRAD	Card Reader Address	TTY/Card Reader Interface Card
CS	Cycle Select	Memory Timing and Control Card
CSCR1, 2	Enable Card Reader Routine ROMs 1 and 2	TTY/Card Reader Interface Card
CSP	Chip Select Panel	Control Panel Interface Card
CVT	Convert Hollerith to Hex Subroutine	In ROM on TTY/Card Reader Interface Card
DB00-15	Data Bits 00-15	Control Panel Interface Card
DI00-15	Data In Bits 00-15	Memory Storage Card
DICTL	Data In Control	Memory Timing and Control Card
DI•EN	Data In and Memory Enable	Memory Storage Card
DINT	Data Interrupt	TTY/Card Reader Interface Card
DO00-15	Data Out Bits 00-15	Memory Storage Card
DOCTL	Data Out Control	Memory Timing and Control Card
DSI0, 1	Data Switch/Indicators 0, 1	Control Panel Interface Card
DTCRD	Data Card Processing Subroutine	In ROM on TTY/Card Reader Interface Card
EN7F	Enable Page 7F	TTY/Card Reader Interface Card
ENA1, 2	Enable 1 and 2	Control Panel Interface Card
ENBL	Enable	- -
ENCRD	End Card Processing Subroutine	In ROM on TTY/Card Reader Interface Card
ENDSUB	End of Subroutine (Panel)	Control Panel Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
EN•MOD0, 1	Memory Enable and Module Select 0, 1	Memory Storage Card
EXEC	Execute	Operators Control Panel
EXHOLD	Extra Hold (Clock 4)	Control Panel Interface Card
GEEO	Teletype Get Character with Echo Subroutine	In ROM on TTY/Card Reader Interface Card
GETC	Teletype Get Character Subroutine	In ROM on TTY/Card Reader Interface Card
HLT	Halt	Control Panel Interface Card
HLTLT	Halt Light	Control Panel Interface Card
HLTS	Halt Switch	Operators Control Panel
HLT+RFSH	Halt or Refresh	Control Panel Interface Card
HSPDIN	High Speed Data In	Teletype Transmitter
IAR	Increment Address Register	Control Panel Interface Card
I/F	Interface	- -
INIT	Initiate	CPU Card
INIT*BB	Initiate * Buffered Twice	Control Panel Interface Card
INTEN	Interrupt Enable	CPU Card
INTEST	Teletype In Test Subroutine	In ROM on TTY/Card Reader Interface Card
INTREQ	Interrupt Request	TTY/Card Reader Interface Card
INTRPTENBL	Interrupt Enable	TTY/Card Reader Interface Card
LDI	Load Immediate	Control Panel Interface Card
LDM	Load Multiple Subroutine	In ROM on TTY/Card Reader Interface Card
LDS	Load Display Latches	Control Panel Interface Card
LM	Load Module	- -
LOCKS	Lock Switch	Operators Control Panel
LPRG	Load Program	Control Panel Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

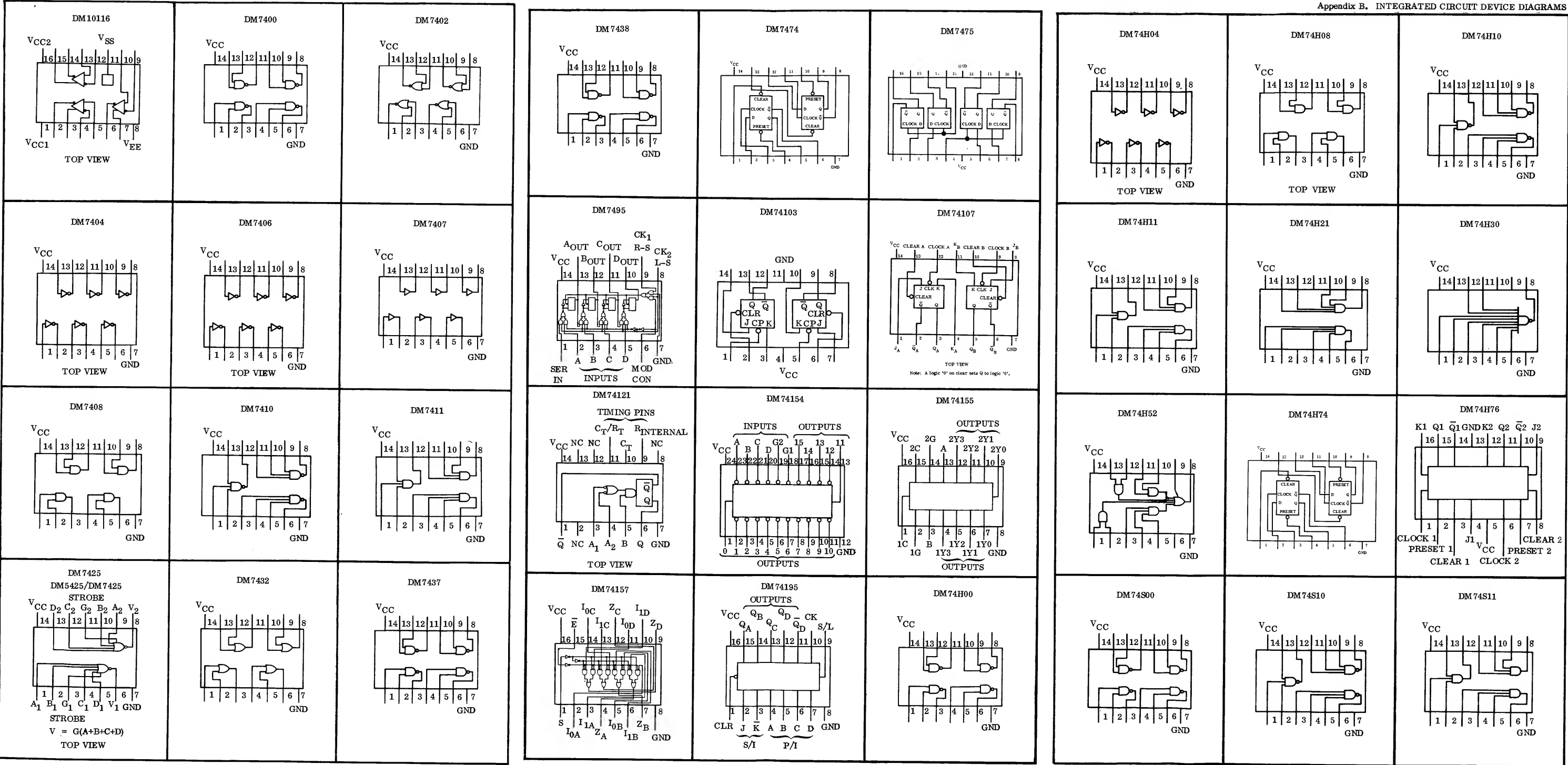
Mnemonic/ Abbreviation	Definition	Source/Reference
LPRGS	Load Program Switch	Operators Control Panel
MAB0-9	Memory Address Bits 0-9	Memory Timing and Control Card
MDI00-15	Memory Data In Bits 00-15	Memory Timing and Control Card
MDIS	Memory Disable	Control Panel Interface Card
MDISFE, FF	Memory Disable, Page FE and FF	TTY/Card Reader Interface Card
MDO00-15	Memory Data Out, Bits 00-15	Memory Storage Card
ME1, 2	Memory Enable 1, 2	Control Panel Interface Card
MEMBSY	Memory Busy	Memory Timing and Control Card
MEMEN	Memory Enable	Memory Timing and Control Card
MESG	Message Printing Subroutine	In ROM on TTY/Card Reader Interface Card
MODSEL0-7	Module Select 0-7	Memory Timing and Control Card
MR/W	Memory Read/Write	Control Panel Interface Card
ODA	Output Data Available	Memory Timing and Control Card
ODIS	Output Disable	Control Panel Interface Card
ORD1-6	Orders 1-6	TTY/Card Reader Interface Card
OUTEN	Output Enable	Control Panel Interface Card
PCHG	Precharge	Memory Timing and Control Card
PD00-15	Peripheral Data Bits 00-15	TTY/Card Reader Interface Card and Control Panel Interface Card
PPP	Programmers Panel Card In Place	Programmers Panel Card
PRGM	Program	TTY/Card Reader Interface Card
PRST	Preset	- -
PUT2C	Send Two Characters to Teletype Subroutine	In ROM on TTY/Card Reader Interface Card
PUTC	Teletype Put Character Subroutine	In ROM on TTY/Card Reader Interface Card
RAM	Random Access Memory	- -

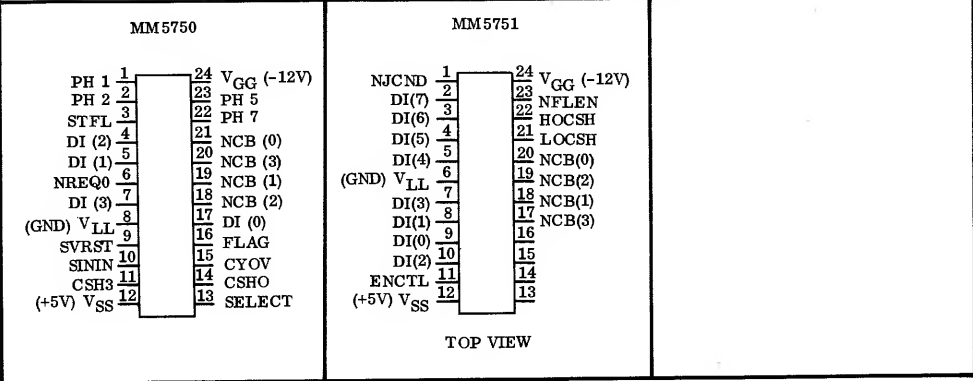
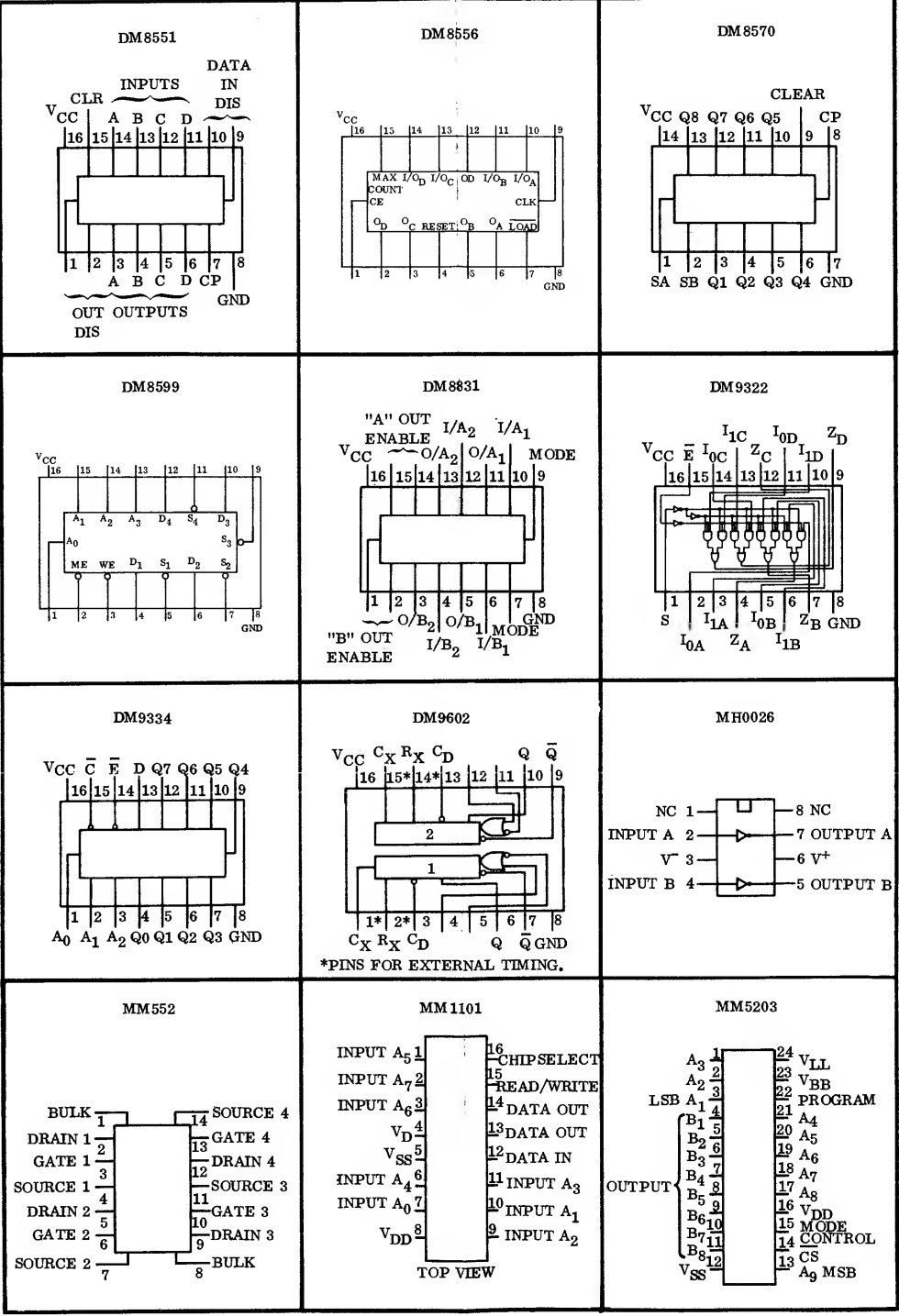
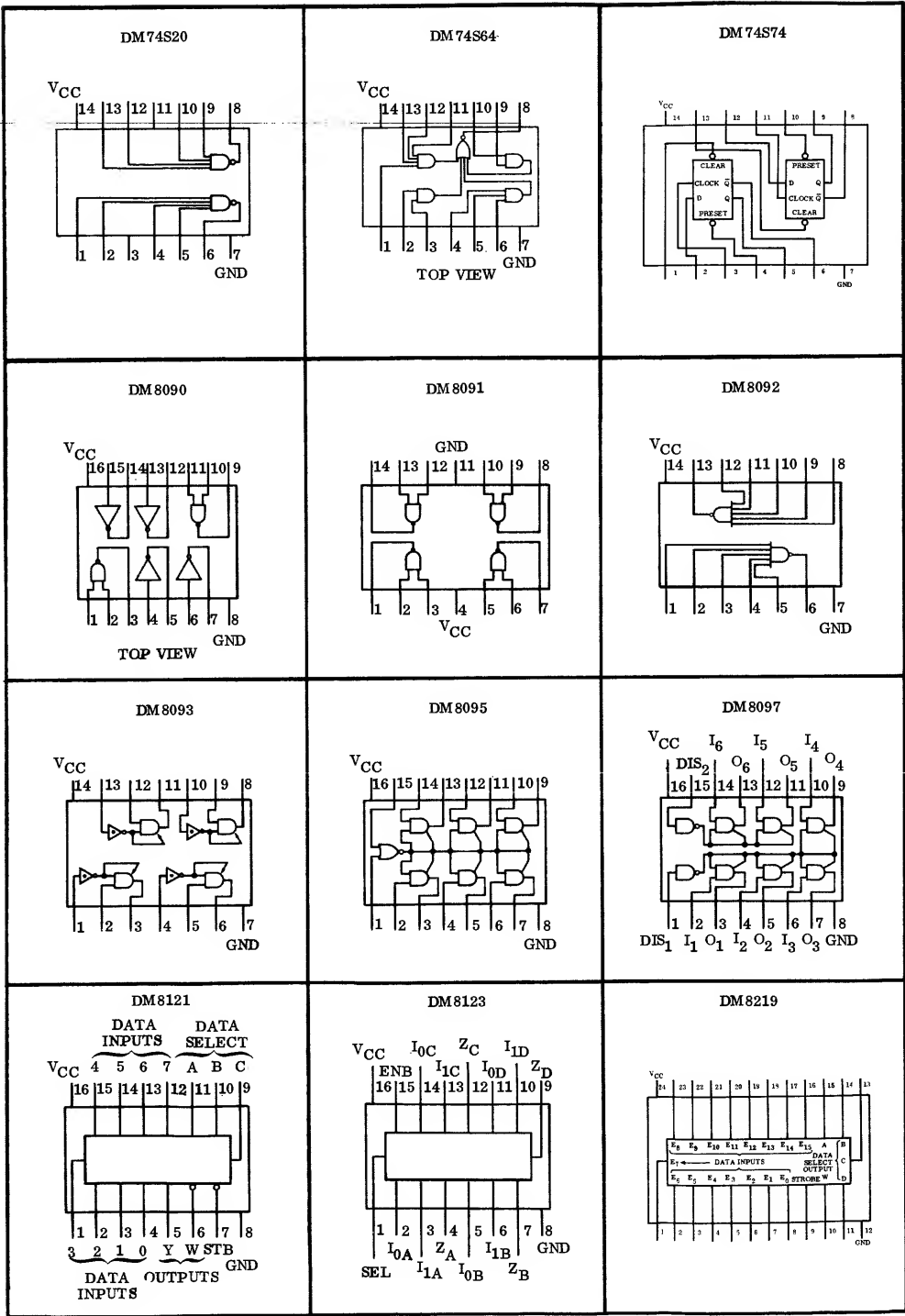
Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
RAMADDR	RAM Address	Control Panel Interface Card
RCP	Read Control Panel	Control Panel Interface Card
RDCOL	Read and Convert Single Column Subroutine	In ROM on TTY/Card Reader Interface Card
RDCRD	Read Card Subroutine	In ROM on TTY/Card Reader Interface Card
RDEN	Read Enable	TTY/Card Reader Interface Card
RESET	Teletype Reset Subroutine	In ROM on TTY/Card Reader Interface Card
RDM	Read Memory	CPU Card
RDMFLG	Read Memory Flag	CPU Card
RDP	Read Peripheral	CPU Card
RDRON	Reader On	TTY/Card Reader Interface Card
RDSW	Read Switches	Control Panel Interface Card
RDWD	Read and Convert 16-bit Word Subroutine	In ROM on TTY/Card Reader Interface Card
RFADR0-4	Refresh Address 0-4	Memory Timing and Control Card
RFSH	Refresh	Memory Timing and Control Card
RFSHPROG	Refresh In Progress	Memory Timing and Control Card
RFSHREQ	Refresh Required	Memory Timing and Control Card
RLT	Run Light	Control Panel Interface Card
ROM	Read Only Memory	- -
ROUTCPAD1	Register Out, Control Panel Address, 1	Control Panel Interface Card
ROWSEL0-3	Row Select 0-3	Memory Timing and Control Card
RPFLG	Read Peripheral Flag	Control Panel Interface Card
R/W(MOD0, 1)	Read/Write (Module 0, 1)	Memory Storage Card
SAV	Save Registers Subroutine	In ROM on TTY/Card Reader Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
SI	Single Instruction	Control Panel Interface Card
SLCT	Select	--
SLCTMOD0, 1	Select Module 0, 1	Memory Storage Card
SPCK	Set Pick	TTY/Card Reader Interface Card
STM	Store Multiple Subroutine	In ROM on TTY/Card Reader Interface Card
SW00-15	Switched Bits 00-15	TTY/Card Reader Interface Card and Control Panel Interface Card
SW1, 2, 3	Switch 1, 2, 3	Operators Control Panel
SYSCLR	System Clear	CPU Card
SYSCLRS	System Clear Switch (INIT)	Operators Control Panel
TDOUT	Transmit Data Out	TTY/Card Reader Interface Card
TMEMEN	Transparent Memory Enable	Control Panel Interface Card
TTY	Teletype	--
TTY1-2	Enable Teletype Routine ROMs 1 and 2	TTY/Card Reader Interface Card
TTYAD	Teletype Address	TTY/Card Reader Interface Card
TTYDIN	Teletype Data In	TTY Transmitter
TTYSTAT	Teletype Status	TTY/Card Reader Interface Card
WP	Write Pulse	Memory Timing and Control Card
WP0, 1	Write Pulse 0, 1	Memory Timing and Control Card
WRM	Write Memory Flag	CPU Card
WRMB	Write Memory Flag Buffered	Control Panel Interface Card
WRMP	Write Memory Peripheral	CPU Card
WRP	Write Peripheral Flag	CPU Card
WRPA	Write Peripheral A	CPU Card







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